Digital Design LU

Lab Exercise 2

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1 Required Reading

- Design flow tutorial
- VHDL modeling slides
- State machine slides
- IP core documentation

2 Task Description

Task 1: Structural modeling In the first exercise you have already learned how to simulate existing VHDL code and extract vital information (like rudimentary timing or transmitted data). In this task we will shift the focus to structural VHDL modeling. Your task is to write a top-level structural VHDL description of a system.

Figure 1 and Figure 2 show how the components need to be connected. The description must be done in VHDL and should contain only structural primitives (component instantiations and concurrent signal assignments). All information needed to wire the IP cores together is contained in the figures.

Add all needed IP cores and your top-level description to a Quartus project. The PLL displayed in the figure is not supplied. You need to generate it using the corresponding wizard within Quartus (see lab documentation). The frequency of the system clock (PLL output) should be 25 MHz.

The generics used in the figures are defined in Table 1. Make sure you use constants in VHDL. Do not set the values directly in the generic map.

Constant	Value
SYS_CLK_FREQ	25000000
SYNC_STAGES	2
VGA_MIN_FIFO_DEPTH	10
DISPLAY_COUNT	2

Table 1: Used generics.

After the PLL is created, add the necessary pin assignments and synthesize the project. Download the resulting bit stream to the FPGA board and make sure, that the system works. Show the result to a tutor and fill out the lab protocol.

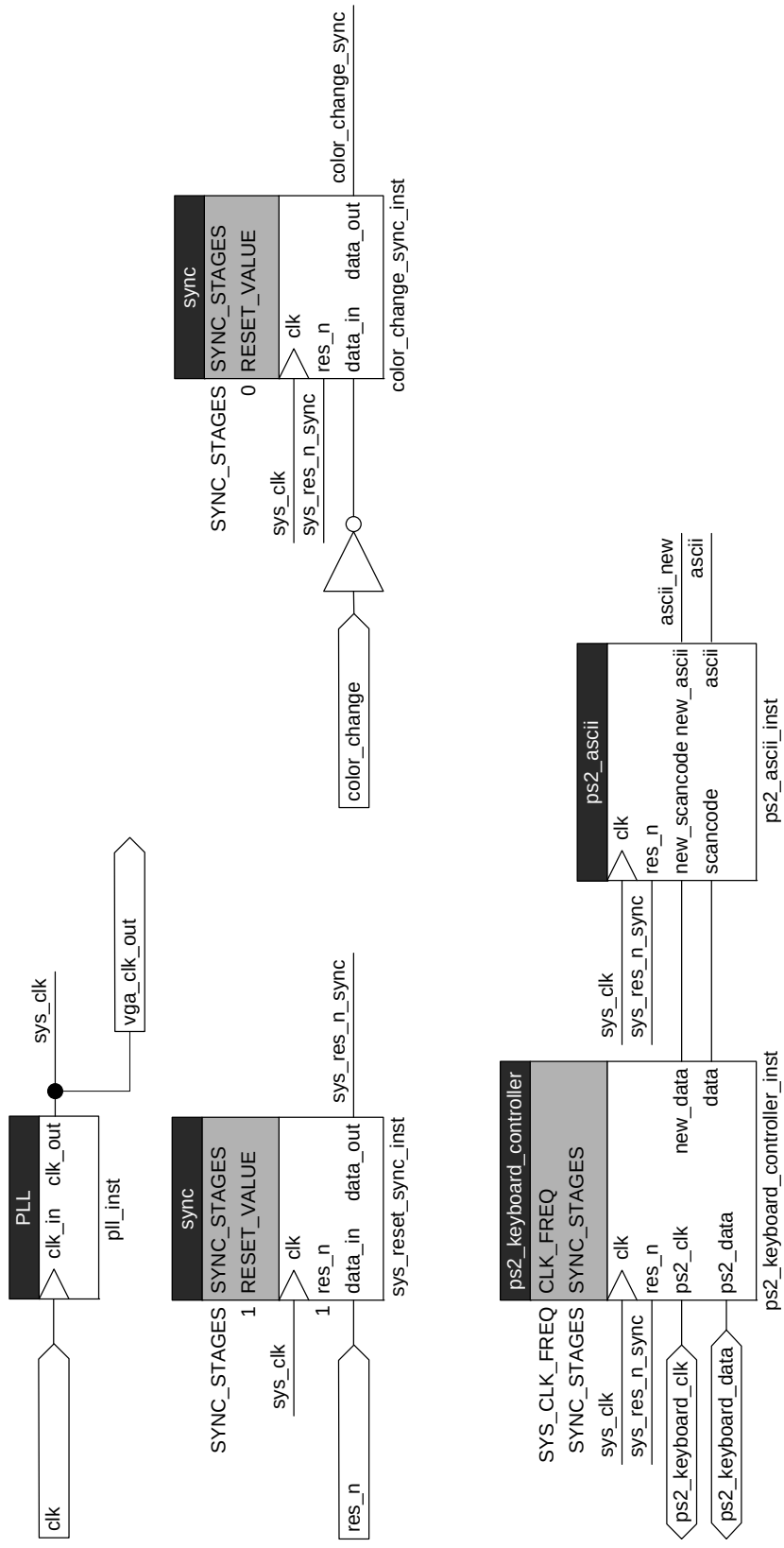

Figure 1: Structural system description (part1).

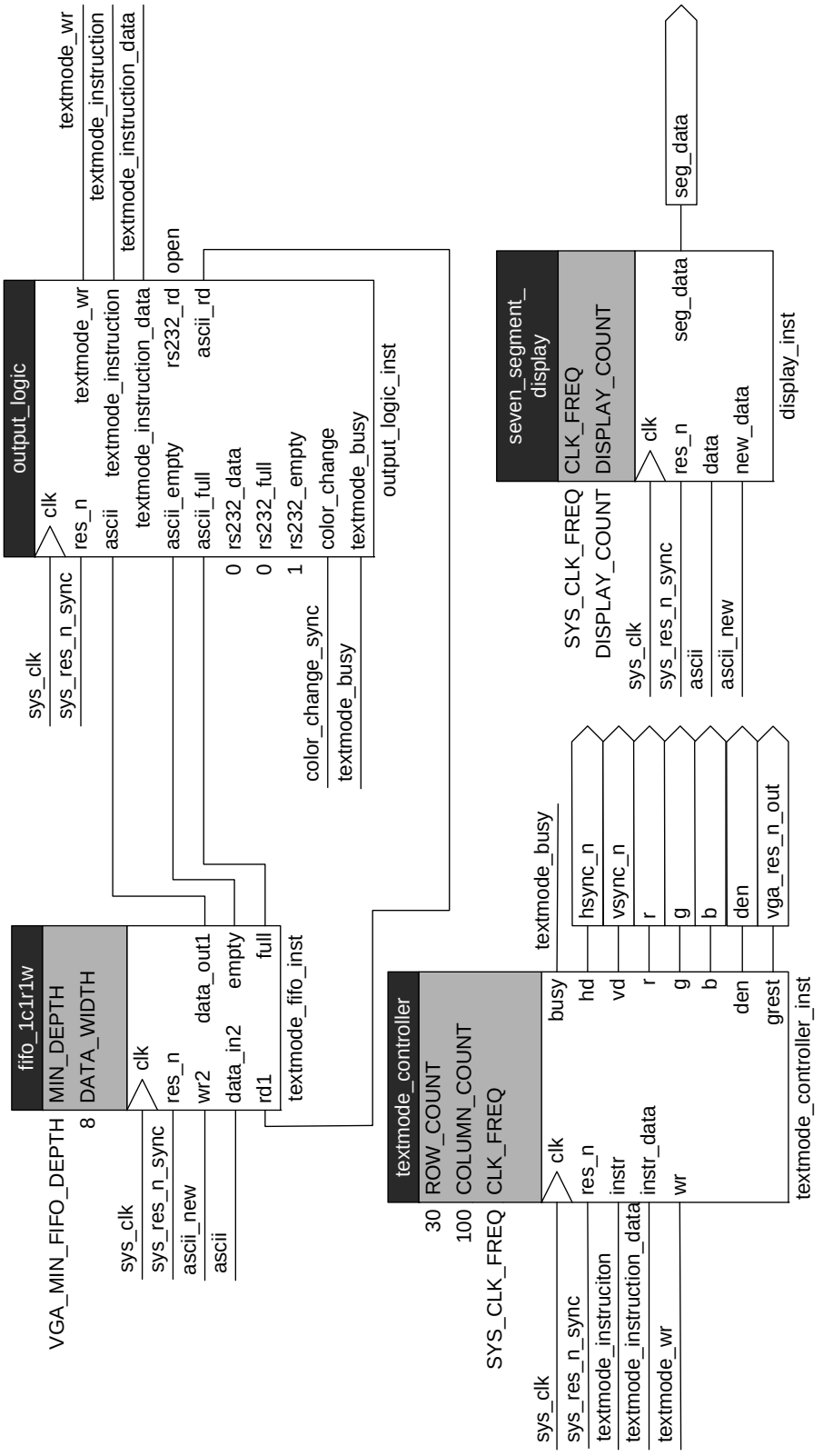

Figure 2: Structural system description (part2).

3 Submission Specification

The results are again handed in via myTI. The deadline is October 31^{st}, 2011, 23:59. Upload a ZIP file containing the following information:

- Your lab protocol as PDF
- The source code of all IP cores
- The source code of the PLL
- The SDC file containing the clock definition
- The source code of your top-level module
- Your Quartus project (don't forget a cleanup!) or a TCL script creating the project (including the pin mappings!)

Make sure the submitted Quartus project is compilable. All submissions which can not be compiled will be graded with zero points!