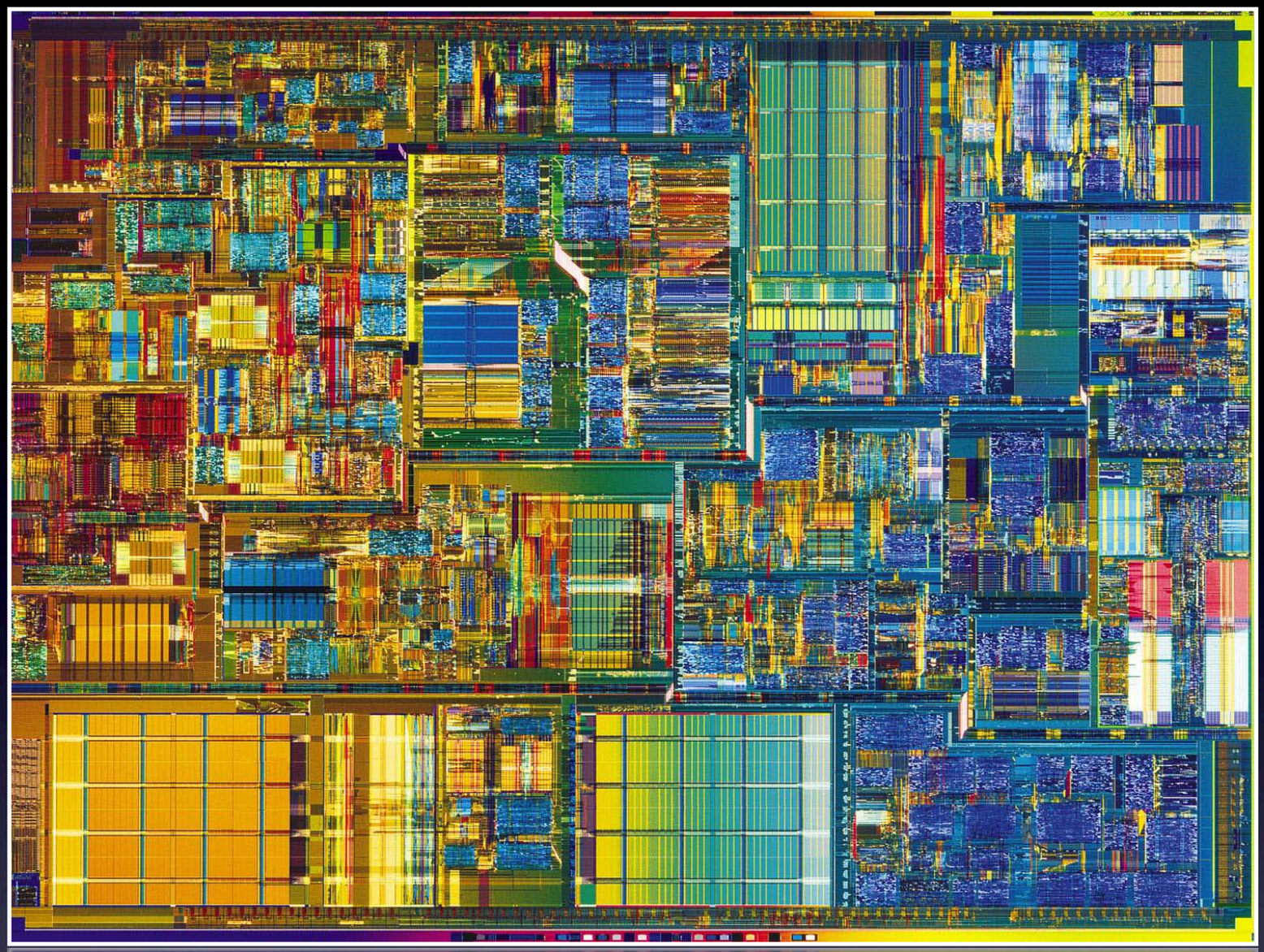


182.695 - LU Digital Design & Computer Architecture (DDCA)

Introductory Talk

Oct. 3rd, 2011

Staff

- Jakob Lechner, Thomas Polzer, Wolfgang Puffitsch, Andreas Steininger
- Stud. Assistant: Andreas Hagmann
- Tutors: Jomy Chelackal, Florian Huemer, Thomas Preindl, Jörg Rohringer, Markus Schütz

Contact

- Tutors in the supervised Lab-Slots
- Email:
  - lechner@ecs.tuwien.ac.at
  - tpolzer@ecs.tuwien.ac.at
  - wpuffits@mail.tuwien.ac.at

LU Digital Design (182.045)

- Previous lecture (old curricula, taught until WS 2010)
- DiDeLu and DDCA are equivalent
- Either DiDeLu or DDCA necessary, not both!
- Only one of the two can be used!

Prerequisites

- Mandatory
  - STEOP
- Recommended
  - VO Digital Design
  - VO Hardware Modeling (this term, parallel to LU)
  - VO Rechnerstrukturen (this term, parallel to LU)

Registration

- Register in TISS
- Register in myTI
- Groups of three people
  - (optional) Enter group suggestions into myTI
- Registration ends Oct. 4th, 12:00!

Syllabus

- Digital Design
  - FPGA design-flow
  - Logic analyzer measurements
  - Structural VHDL modeling
  - Behavioral VHDL modeling
  - State machine design
- Computer Architecture
  - Simple pipelined microprocessor

The Lab

- TILAB: Room no. 2
  - TreitIstraße 1-3, Hochparterre
- Accounts and access cards
  - Handed out in supervised lab slots
  - Upload a photo to myTI (Until Oct. 4th, 12:00)
  - Must be claimed before Oct. 19th, otherwise you will be unregistered from the course!
  - Working in the lab only allowed after you have claimed your account!

The Lab

- Supervised slots by tutors
  - Registration via myTI required (on group basis)
    - Register ASAP!
- Outside of supervised slots
  - First come first serve policy

Working environment

- Work directly in the lab
- or at home
  - Remote SSH shell (X-forwarding) to the lab
    - Download to FPGA board forbidden!
  - Locally on your own machine
    - Tools freely available (see lab homepage)

Organization

- Four Digital Design exercises
- Midterm exam (individual)
- Two Computer Architecture exercises
- Final exam (individual)

Digital Design

- Exercise I
  - Get to know the tools (ModelSim, Quartus, Logic Analyzer)
  - Working VHDL code provided (Simulate, Build, Analyze)
- Exercise II
  - Component integration (Structural VHDL modeling)
- Exercise III
  - Behavioral VHDL modeling
  - State machine implementation based on provided state chart
- Exercise IV
  - Design and implementation of a state machine

Midterm Exam

- Similar tasks as in lab exercises I - IV
- Measurements
  - Simulation
    - Logic analyzer
- Create a structural VHDL design
- Create a behavioral VHDL design
  - e.g. coding a state machine

Computer Architecture

- Exercise V
  - Implementation of a basic, simplified MIPS processor (Mini-MIPS)
  - No hazard handling!
- Exercise VI
  - Adding hazard handling to the MIPS processor
  - Implementation of an advanced processor feature
    - e.g. exceptions or interrupts
  - Extra points for implementation of an additional advanced feature

Final exam

- Tasks similar to exercises V and VI
  - e.g. coding an ALU or resolve a pipeline hazard
- Theoretical questions based on lab exercises V and VI

Exercise Workflow

- Solve task assignments as group
- Write a protocol based on given templates
- Submit required files via myTI before submission deadline
- Discuss the implementation and protocol with a tutor (resubmission possible before deadline!)

Grading

Task	Percentage
Lab exercises	30%
Midterm exam	35%
Final Exam	35%

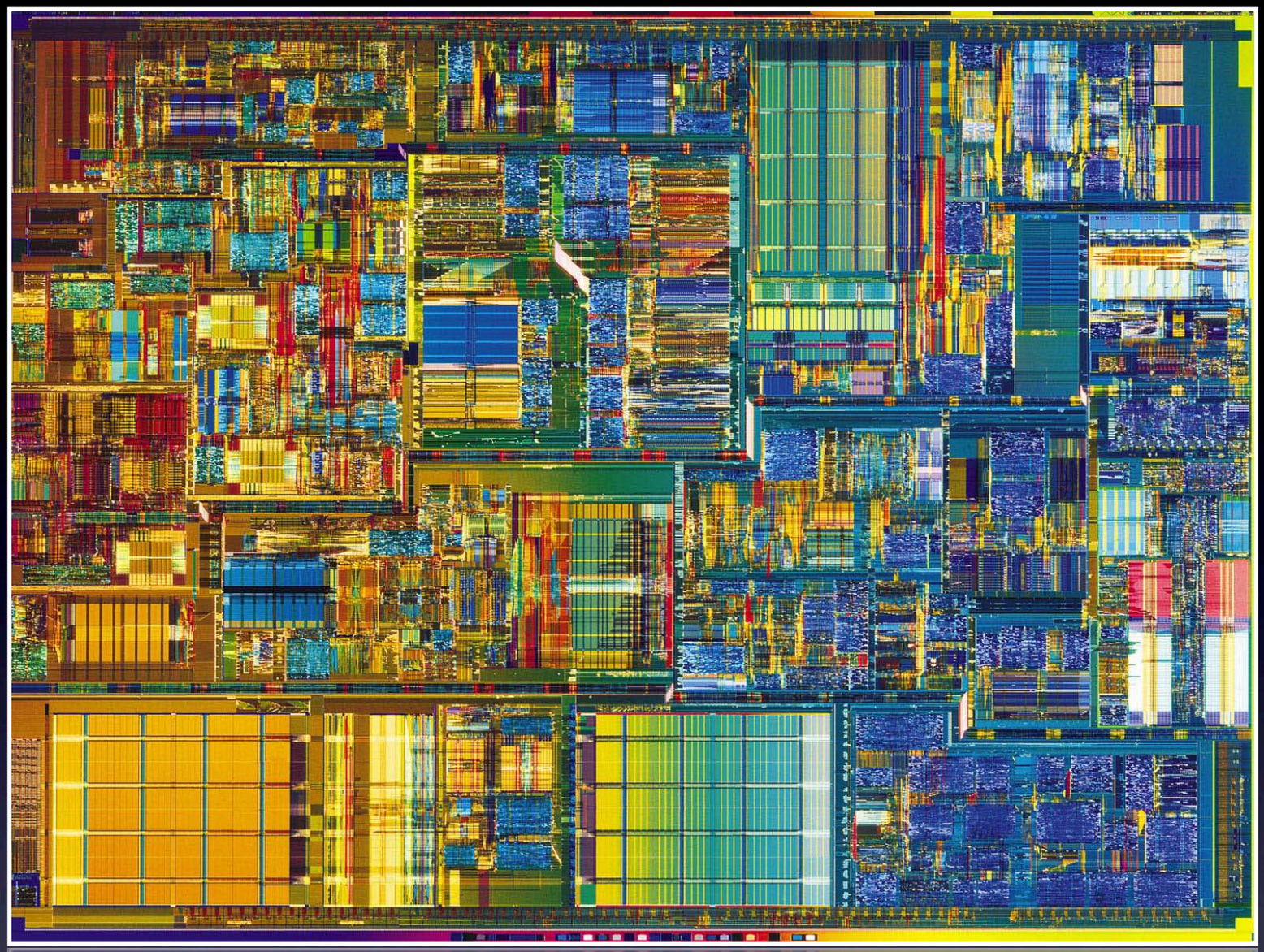
Grade	Percentage
S1	89% - 100%
U2	76% - 88%
B3	63% - 75%
G4	50% - 62%
N5	<50%

Schedule

Date	Event
until Oct. 4th, 12:00	Registration via TISS and myTI
Starting Oct. 5th	Registration for lab slots
Oct. 5th	Start of lab
Oct. 19th	End of account pickup
Oct. 19th	First exercise due
Oct. 31st	Second exercise due
Nov. 11th	Third exercise due
Nov. 25th	Fourth exercise due
Nov. 28th - Nov. 30th	Midterm exam
Dec. 19th	Fifth exercise due
Jan. 20th	Sixth exercise due
Jan. 23rd - Jan. 27th	Final exam

Optional Literature

- Computer Organization and Design
  - David A. Patterson & John L. Hennessy
- Computer Architecture, A Quantitative Approach
  - John L. Hennessy & David A. Patterson



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