# Digital Design and Computer Architecture 182.695

Florian Huemer & Sebastian Wiedemann & Dylan Baumann

March 7, 2024

# The DDCA Course Team



- Teaching Staff
  - Florian Huemer
  - Sebastian Wiedemann
  - Dylan Baumann (Student Assistant)
- Tutors
  - Andreas Lukitsch
  - Daniel Blattner
  - Jakob Buchsteiner
  - Norbert Tremurici

# Registration



- Register in TISS! (Now!)
- Registration ends today after this talk
- On Monday (11.03.2024) you will be added to the TUWEL course automatically

# Contact and Platforms



- TUWEL Course
  - Submission and points tracking
  - Sign-up for lab exams
- TU Chat Channel (link in TUWEL)
  - General course communication (e.g., announcements)
  - Questions from your side
- Zoom (link will be posted in TU Chat)
  - Tutor slots
  - Q & A sessions
- TU Gitlab (assignments and course material)
- E-Mail (for organizational questions only)
  - fhuemer@ecs.tuwien.ac.at

# Formal Prerequisites



- Mandatory
  - STEOP
- Strongly Recommended
  - VO Digital Design ($3^{rd}$ semester)
  - VO Computer Architecture
    - Normally in parallel to the DDCA course, but **not offered** in this summer term!
    - We expect you to know the computer architecture course material
- In Parallel
  - VO Hardware Modeling

# What prior knowledge do we expect?



- Basic programming knowledge (especially C)
- Digital Design Basics
  - Combinational logic, basic gates (AND, OR, XOR, etc.)
  - Sequential components (flip-flops, latches)
  - Memories (RAM/FIFO)
  - CMOS Basics (driver, tri-state, pullup/pulldown resistors, etc.)
  - Synchronizers/Metastability
- State Machines
  - Registers, next-state/output logic
  - Moore vs. Mealy
- Basic pipelining concepts
- Processor architecture

# Content and Learning Objectives



- Digital Design
  - FPGA design-flow
  - Structural VHDL modeling
  - Behavioral VHDL modeling
  - State machine design
  - Pipelining
- Simple measurements using a mixed-signal scope
- Computer architecture: Simple (pipelined) RISC-V microprocessor

# Course Procedure



- Course is divided into 4 subject matters $\Rightarrow$ Levels 1 to 4
- (Level 0)
  - Not a “real” level/no exam
  - Introduction to the tools and lab environment
- Level 1
  - VHDL basics, combinational and simple sequential designs, simple FSMs
  - Basic testing
- Level 2
  - Understanding timing diagrams/interface protocols, external interfaces
  - Advanced FSMs
  - Advanced testing (e.g., file IO)
- Levels 3 & 4
  - Pipelined designs, RISC-V, processor pipeline

# Course Procedure (continued)



- Each Level
  - lasts for roughly 4 weeks
  - ends with a lab exam
- Exam Dates

| Event | | Date |
|---|---|---|
| Level 1 Exam | Tuesday | 09.04.2024 |
| Level 2 Exam | Friday | 03.05.2024 |
| Level 3 Exam | Monday | 03.06.2024 |
| Level 4 Exam | Friday | 28.06.2024 |

- Programming exercise on the lab computers
- Multiple exam slots spread out over the exam days

# Course Procedure (continued)



- To be eligible to take an exam you need to collect enough **Skill Points** for that level
- Solve (small) tasks and present them to a tutor in the lab
- Tutors
  - provide you with feedback
  - check if you can explain your solution
  - award the Skill Points
- If you cannot explain your solution $\Rightarrow$ Special exercise interview with teaching staff
- Skill Points **do not** count towards your final grade

# Course Procedure (continued)



- Tasks prepare you for the exams
- Skill Points are the way **for you to show us** that you engaged with the course material
- The target Skill Points value is not very high
- Depending on your previous knowledge and your proficiency with the topics, achieving just this minimum **does not guarantee success** at the exams
- It is **your responsibility** to
  - make a reasonable selection of the tasks you want to work on and present (i.e., cover all topics)
  - practice for the exams

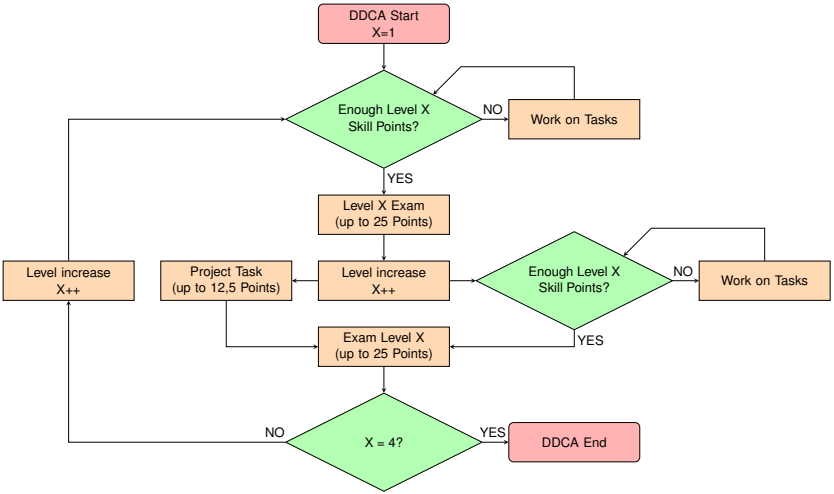
# Course Procedure (continued)



- Additionally there will be 2 **Project Tasks**
- Project Tasks
  - are available in Level 2 and Level 4
  - have a wider scope than regular tasks
  - bring enough Skill Points for that particular level
  - entail a longer exercise interview (appointment in TUWEL)
  - must be submitted in TUWEL
  - are **graded** and count towards the final grade

# Your Path through the DDCA Course





# Points and Grades



- 5 partial achievements
  - 4 individual exams ($E_x$) $\Rightarrow$ 25 points
  - Project Tasks (both together) ($P_1, P_2$) $\Rightarrow$ 25 points
- We discard the worst result and add up the rest
  - You can miss an exam and still get 100 points
  - There won't be any additional exams (i.e., no "Nachtests")
  - Final points $= sum(E_1, E_2, E_3, E_4, P_1 + P_2) - min(E_1, E_2, E_3, E_4, P_1 + P_2)$
- Grades (max. Points = 100)

| Grade | Points |
|---|---|
| S1 | $\geq 89$ |
| U2 | $\geq 76$ |
| B3 | $\geq 63$ |
| G4 | $\geq 51$ |
| N5 | $< 51$ |

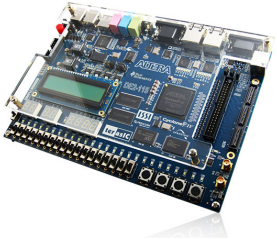
# Learning Support



- Tutor-supervised lab time
  - 4 hours per day, 4 days per week, see TUWEL for exact time slots
  - Also in the Easter holidays (might be partially remote)
  - First come, first served principle
  - You can also ask tutors or present your work remotely via Zoom
- Q&A sessions at the beginning of the semester in conjunction with the Hardware Modeling course
- TU Chat Channel
  - Questions can be asked any time
  - We try to answer them as soon as possible
  - Try to put your question into a single message
  - If you need multiple message, start a thread

# Target Platform and Design Software

- Hardware Platform
  Terasic DE2-115 FPGA Development Board (Intel Cyclone IV FPGA)




- Design Software
  - Intel Quartus 22.1 (FPGA sSoftware)
  - Siemens QuestaSim 22.4/ModelSim 20.1 (digital simulation software)
  - GHDL/GTKWave (open-source simulator)

# Local Working Environment




- TILab in Treitlstaße 3/Hochparterre, Raum 1+2
- 9 computers with FPGA boards and monitors as well as mixed-signal oscilloscopes in Raum 1
- 9 additional computers without FPGA hardware in Raum 2
- Open during normal university opening hours
- See TILab website for current occupancy
- Check for special dates, where the lab might be closed (`https://www.tilab.tuwien.ac.at/timetable.shtml`)

# Local Working Environment



# Remote Working Environment Options



- Virtual Machine Image
  - AlmaLinux 9 (same OS as in the lab)
  - Quartus Lite, ModelSim Intel Edition, GHDL/GTKWave preinstalled
  - Download link in the assignment
- Locally on your own machine (**not recommended**)
  - Free versions of tools available online
  - ModelSim Intel Version 20.1 is the last one that does not require you to register for a license
  - **Be sure that your work compiles in the lab!**
- Remote SSH access to TILab computers
  - Caution: X-forwarding possible, but might be slow (not recommended)

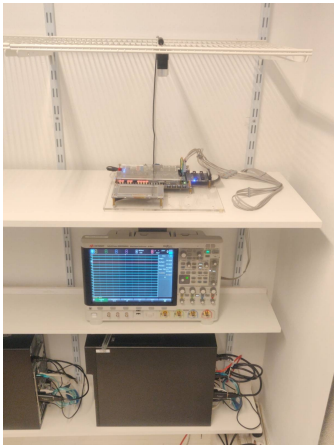
# Hardware access/Remote Lab



- The Remote Lab offers you remote access to FPGA boards and an oscilloscope via
  - simple command-line tools or
  - a web interface
- Video tutorial in the course material
- Advantage: Open 24/7
- All tasks can be completed in the Remote Lab!

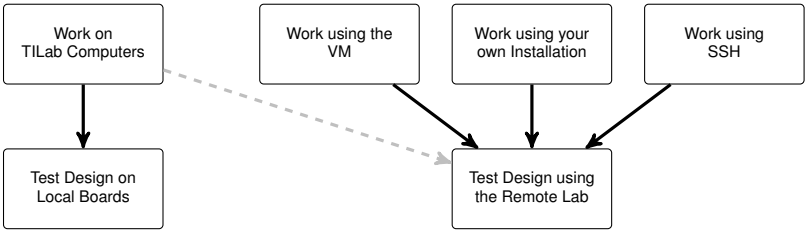
# Remote Lab





# Working Environment Options





# Lab Study



- In 2022 we won the “Digital Teaching Award” at the Best Teaching Awards of the TU for our Remote Lab concept
- We would like to
  - further improve our teaching methods and lab courses and
  - publish our concept/software tools to a wider audience
- To achieve this and prove that our approach is viable, we would like to study how course participants
  - interact with the EDA software
  - use the Remote Lab compared to the local lab

# Lab Study



- Data collection consent form in TUWEL course
- Data is anonymous and only stored on the TILab infrastructure (no cloud involved) **The participation in this study is absolutely voluntary. It will not have ANY impact on your final grade.**
- Giveaway: Study participants (that successfully complete the course) have the chance to win one of two development boards
  - BeagleBone Black
  - Arduino Mega 2560

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