Memory Models

Computer Systems

Johann Blieberger

Sequentially Consistent World

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- For general considerations (correctness of a program, . . .) one must therefore assume **all** interleavings as possible.

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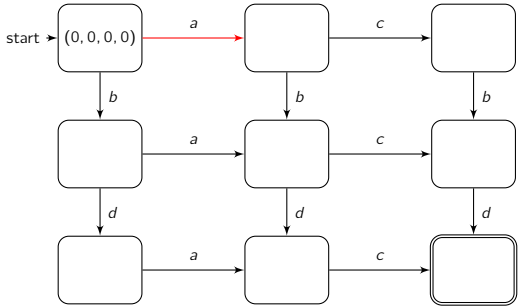

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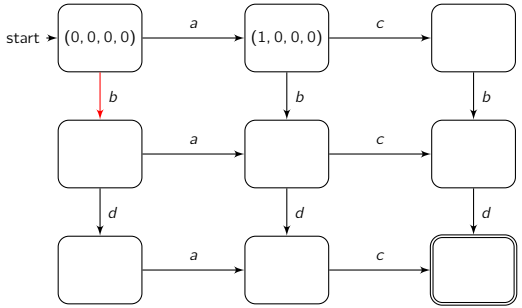

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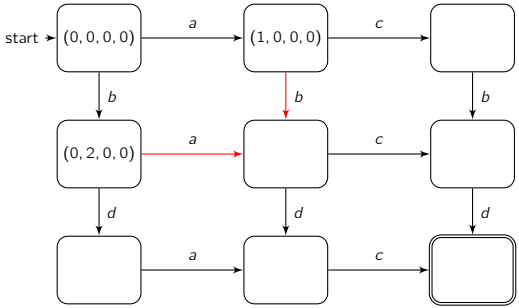

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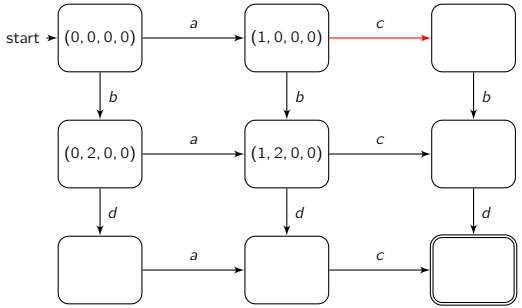

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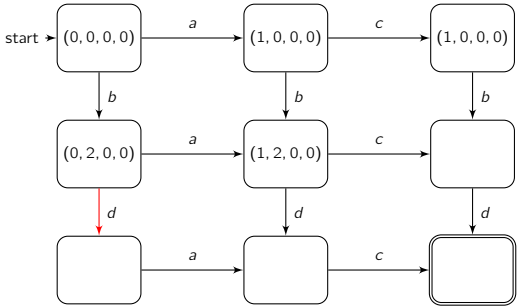

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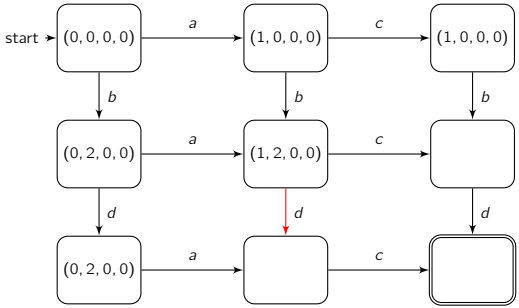

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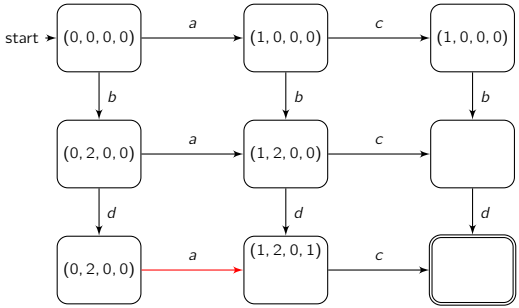

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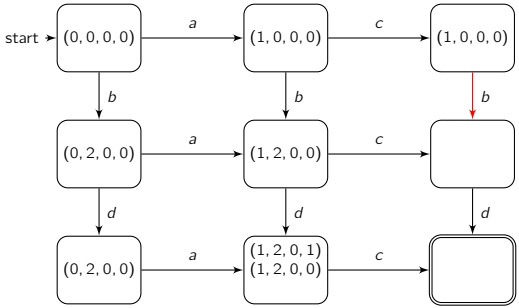

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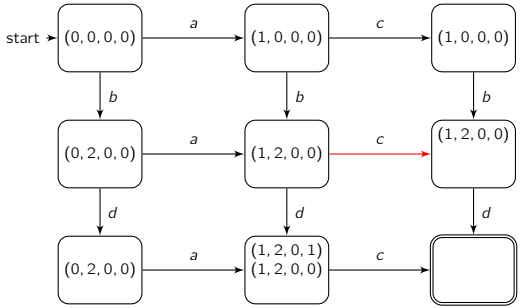

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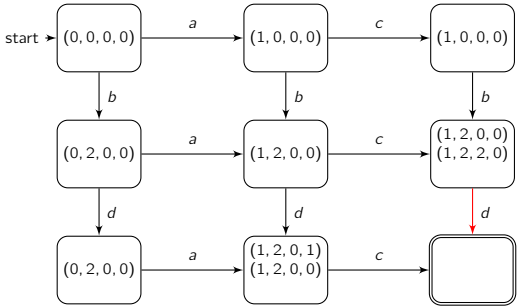

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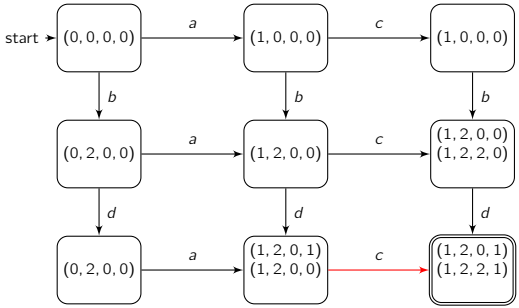

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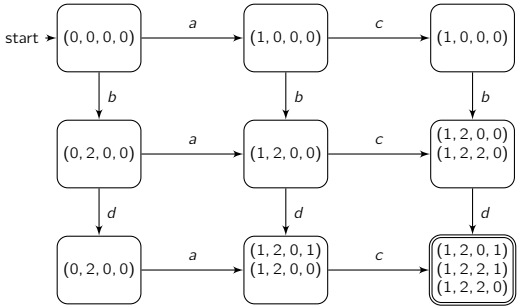

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$\longrightarrow$ **Sequentially Consistent Memory Model (SC)**

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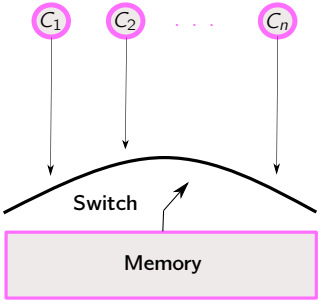

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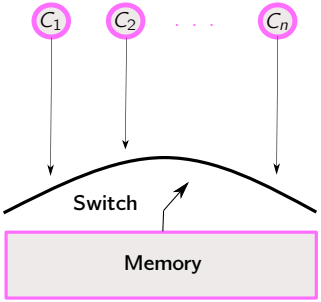

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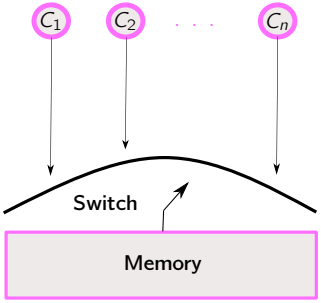

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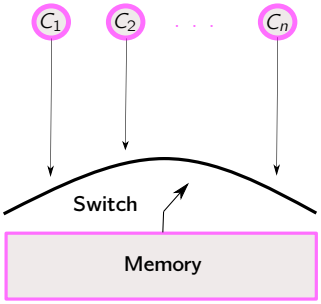

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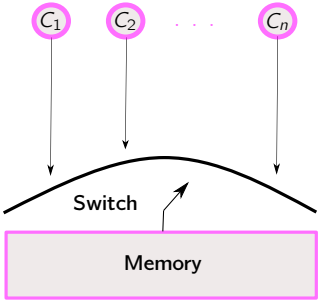

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Note: This is not what the hardware does! But it can serve as a model for how we want to think about hardware.

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- **Question:** If T_1 first copies the second half, and then T_2 reads both halves: What value does T_2 get?

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- Programming languages also know **atomic types** and **operations** on atomic variables.
- When multiple threads access the same memory area (variable) simultaneously, this is called a **Data Race**.

Atomics

- We have seen: When multiple threads access common memory cells (variables), it may be necessary to guarantee that operations on variables are executed **atomically**, i.e., **indivisibly**.
- This can only be guaranteed by the **hardware** (CPU).
- All common CPUs offer such **atomic operations** as **instructions**.
- Programming languages also know **atomic types** and **operations** on atomic variables.
- When multiple threads access the same memory area (variable) simultaneously, this is called a **Data Race**.

. . . we will come back to this later. . .

Synchronization and Communication

Producer – Consumer

- Task: A piece of data should be safely transferred from one thread to another thread.

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- T_1 sets flag F=1.
- T_2 reads F. If F=0, it continues to read F.
- When T_2 reads F=1, it can read D "safely".

Producer – Consumer

As source code:

	T_1	$(D, F, X) = (0, 0, 0)$		T_2
d:	`D := 42;`		if:	`if F=0 then goto if;`
f:	`F := 1;`		x:	`X := D;`

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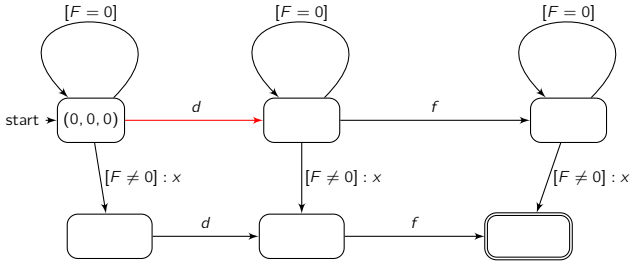

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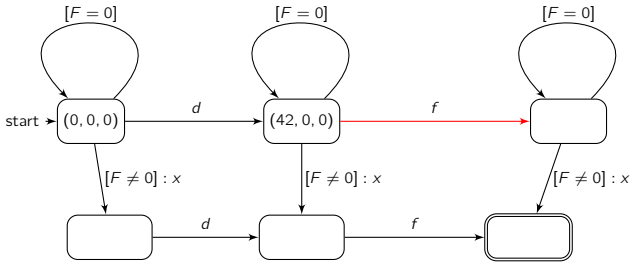

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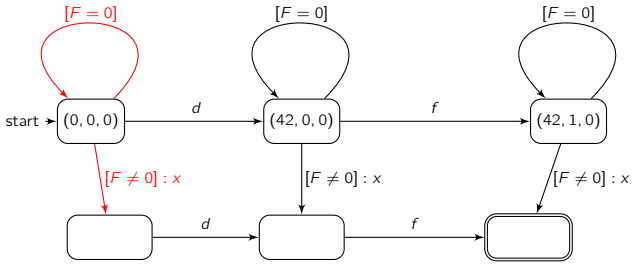

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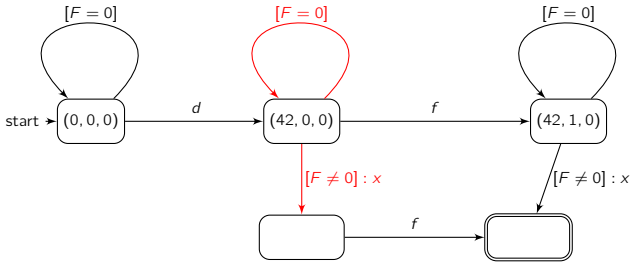

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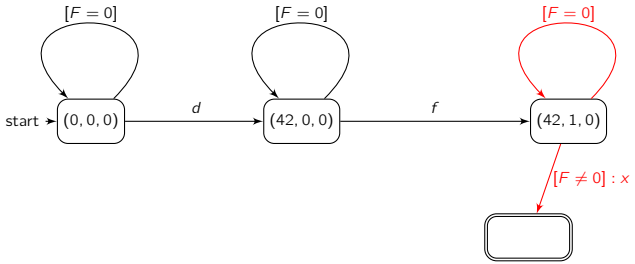

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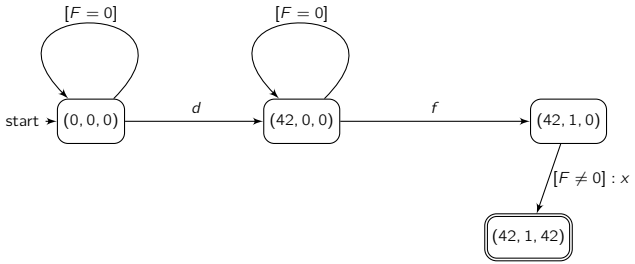

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Program & Execution Order

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- In addition to the atomic variables, executing the instructions in **program order** was recognized as a prerequisite for the Sequentially Consistent memory model.

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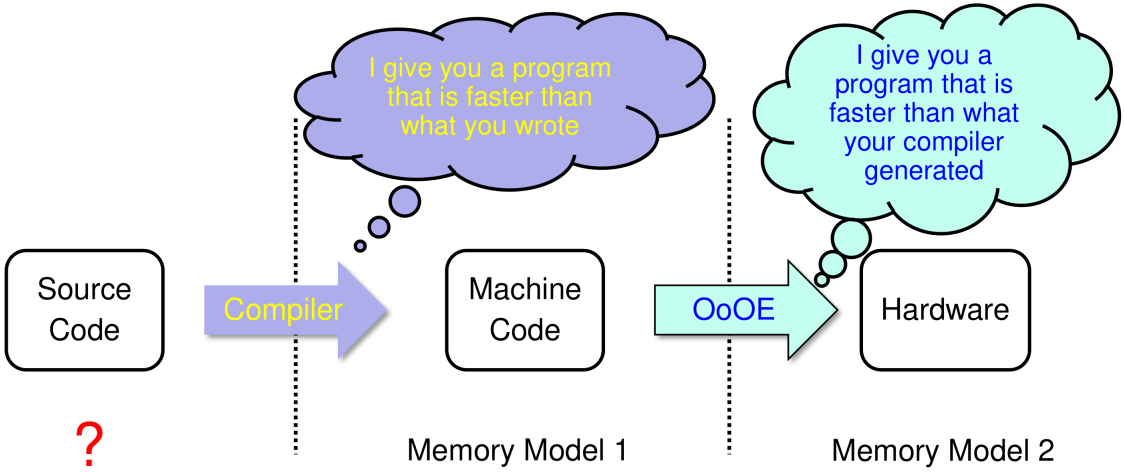
- Modern computer architectures do not guarantee executing the instructions in program order!

Program Execution Hierarchy

Changing the Execution Order



Program Execution Hierarchy

- Hierarchy in program execution:

Level	(Re-)Ordering

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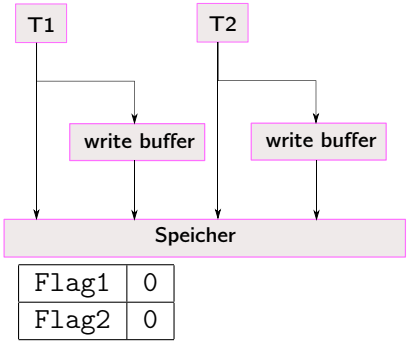
- Programmers (Computer Scientists) must **know** and **consider** that **Program Order** $\neq$ **Execution Order (PO** $\neq$ **EO)**
- **Attention**: Instructions from the calling and called subroutine can be "mixed".

SC Violation – Architecture without Caches



Initial: `Flag1 = Flag2 = 0`

```
T1:
Flag1 := 1;
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- CPU-Cores have **Write-Buffer**

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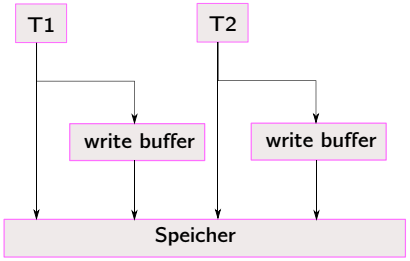

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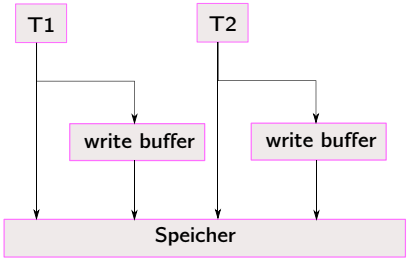

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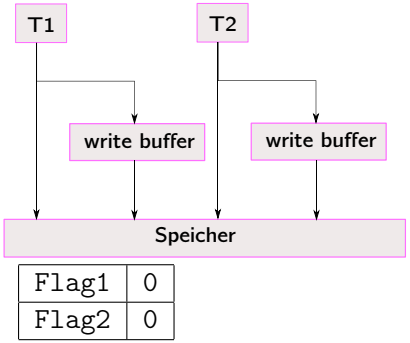

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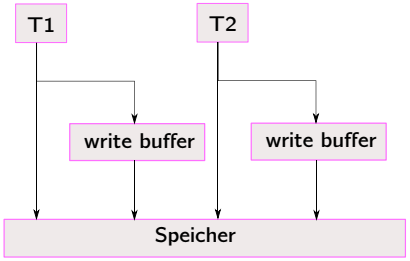

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- **Attention: Read** operations can overtake write operations in the Write-Buffer

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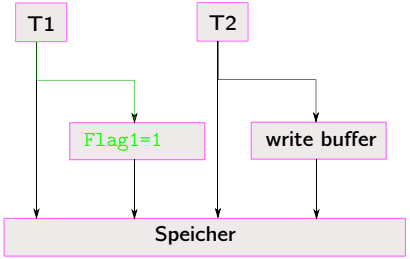

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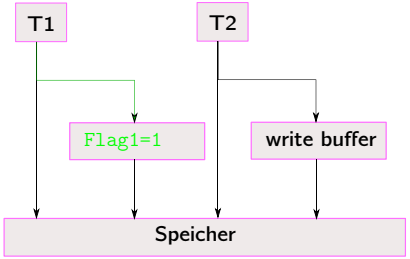

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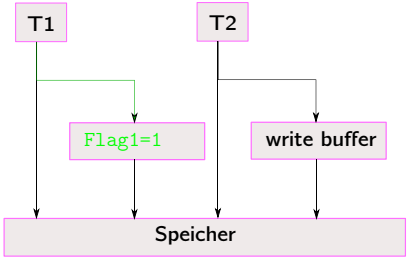

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- there it cannot be seen by T2
- In memory, `Flag1` still has the value 0

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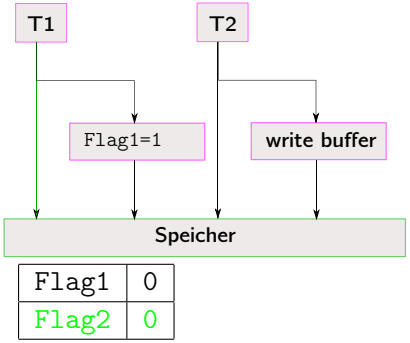

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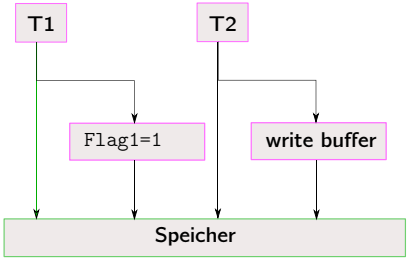

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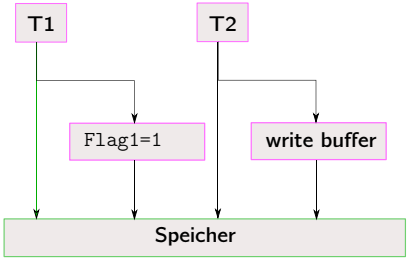

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- Read operation arrives in memory before write operation
- this is the **1st** operation in memory order

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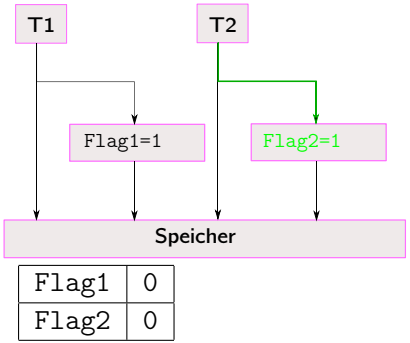

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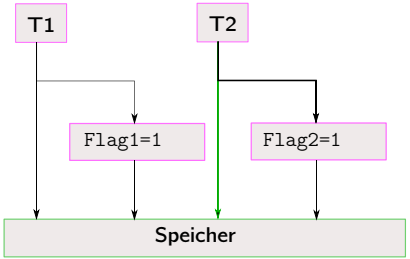
- T2 write operation of `Flag2` goes into the Write-Buffer

SC Violation – Architecture without Caches



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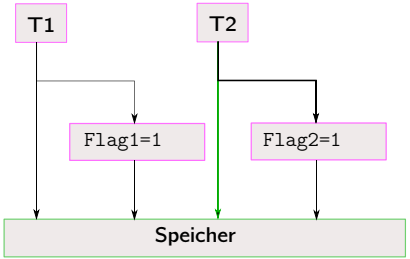

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- T2 read operation of `Flag1` overtakes the Write-Buffer
- This is the **2nd** operation in memory order

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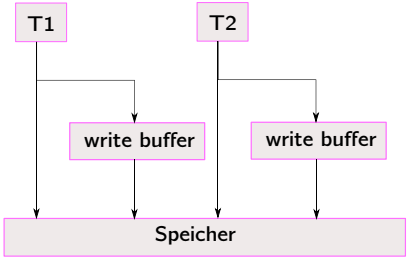

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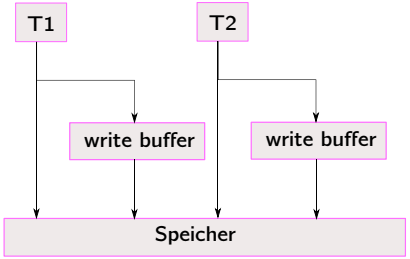
- Due to the Write-Buffer, the SC order (Write(`Flag1`), Read(`Flag2`), Write(`Flag2`) and Read(`Flag1`)) is different from the memory order (Read(`Flag2`), Read(`Flag1`), Write(`Flag1`) and Write(`Flag2`))

SC Violation – Architecture without Caches



Flag1	0
Flag2	0

Initial: `Flag1 = Flag2 = 0`

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T1:                    T2:
Flag1 := 1;            Flag2 := 1;
if Flag2 = 0 then      if Flag1 = 0 then
-- critical            -- critical
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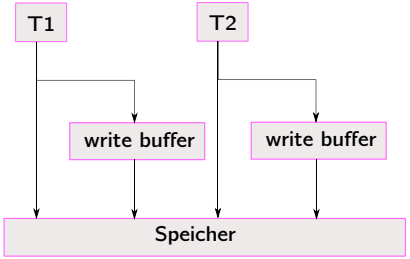

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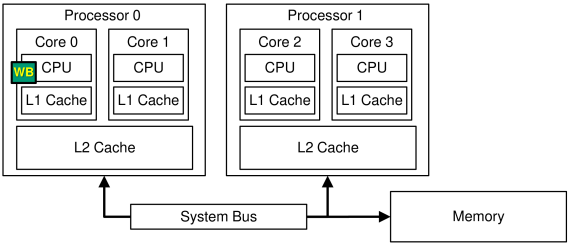
- Is there another possible memory order in this example?

SC Violation – Architecture with Private Caches



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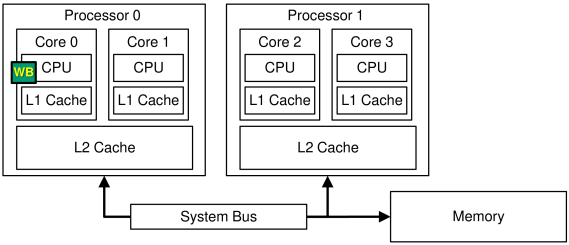

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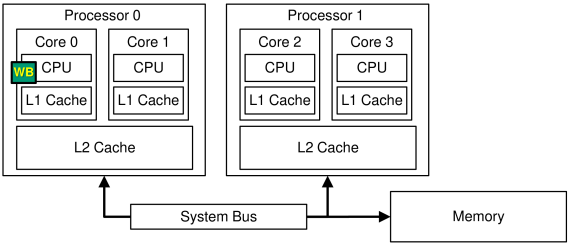

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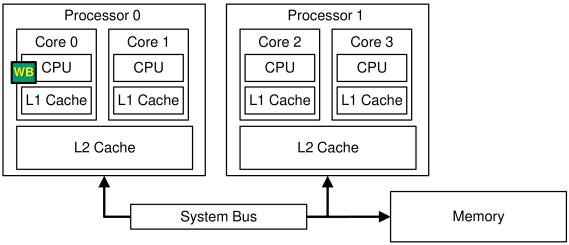

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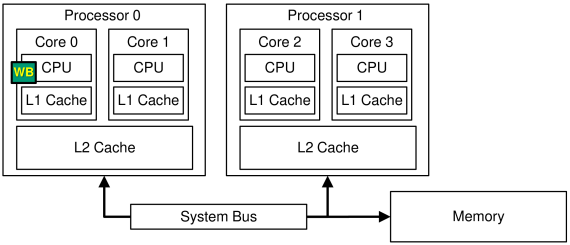

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- **Write** operations must happen immediately; if one core can observe the result of a write operation, then **all** cores can
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c:	`C := B;`		d:	`D := A;`
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- **Now the result $(A, B, C, D) = (1, 2, 0, 0)$ is possible!**

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- $\longrightarrow$ **Relaxed Memory Model** ...
- ... has problems. We will see what those are shortly ...

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a: `A:=1;`	b: `B:= 1;`	c: `C := A;`	e: `E := A`
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- T_3 sees C=1 and D=0, therefore he concludes that $a < b$.

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- T_4 sees E=0 and F=1, therefore he concludes that $b < a$.
- Main cause: f is executed before e and d before c.

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- **The simplest form of communication and synchronization does not work in the Relaxed Memory Model!**

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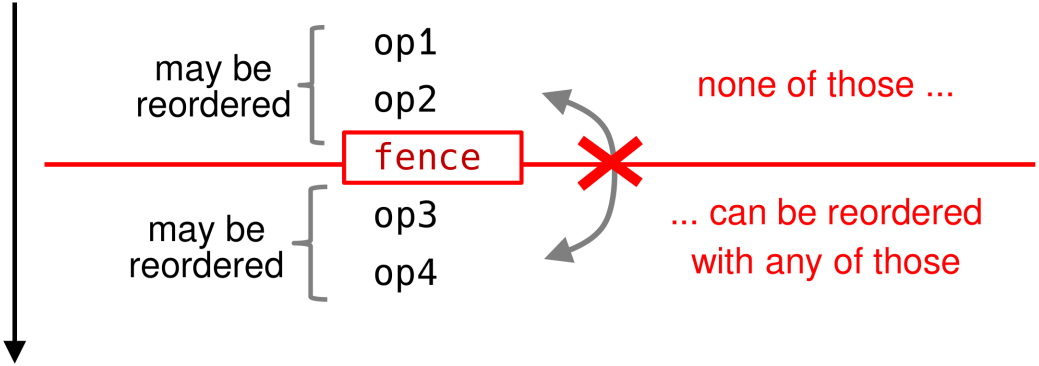
- Modern computer architectures offer so-called **Memory-Fences** (Memory Barriers).
- Moving instructions across Memory-Fences is prohibited.



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Note: Automatic placement of Memory-Fences is not possible (undecidable problem)!
Equivalent to the Halting Problem
(There is no program that can automatically detect infinite loops in programs.)

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Memory Models

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- Programming languages must describe the interactions between threads that take place over memory, and how shared data can be defined and used (interface to the programmer).

Memory Model Operations

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exchanges the values of the two atomic variables `atomic_var1` and `atomic_var2`, where the Memory Order is specified as: `SC`, `Release_Acquire`, or `Relaxed`.

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The programmer must know what s/he is doing!

Producer – Consumer (Release-Acquire Version)

	T_1	$(D, F, X) = (0, 0, 0)$
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f:	`atomic_store(F,1,Release);`	

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- Responsible for the correct use of SC, RA, Relaxed: Programmer/Computer Scientist.

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(. . . more on the topic of performance later . . .)

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- There should be no further instructions before and after the given instructions that can be reordered.

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	T_1
z:	`Z := 15;`
y1:	`Y := 11;`
a:	`atomic_store(A,1,Release);`
	T_2
if:	`if atomic_load(A,Acquire)`$\neq$`1 then goto if;`
y2:	`Y := Z;`

- Initially `A = 0`

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- y1 also cannot be moved behind a, otherwise the value that Y received in y2 could be overwritten.

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- Alternatively: relax a2, not a1?

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Memory Models – Spectrum of Common Architectures

adapted from https://preshing.com/20120930/weak-vs-strong-memory-models/

Blocking Wait

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- Alternative: **Blocking Wait**.

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Counter, initialized to 1
Two operations:

Lock: Decrease counter by 1.
If counter ≥ 0, thread may continue execution.
If counter < 0, enqueue thread in a waiting queue
& stop execution.

Unlock: Increase counter by 1.
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Race condition!

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Memory Fences may be required to prevent code from the Critical Section (between Lock and Unlock) from "wandering out".

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- The “simultaneous” access should be prevented by a semaphore S.

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Although P_1 can continue executing, it is possible that the behavior will not be correct due to the "hidden" modification in shared memory.

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- LL/SC operations are supported by DEC Alpha, PowerPC, MIPS, ARM, RISC-V, ...

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- no nesting of LL/SC operations

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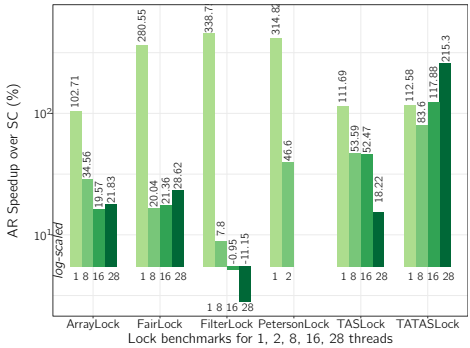
- Non-Blocking more than 100 times faster than Blocking

Performance Gain Intel x86 through SC→AR-Relaxation

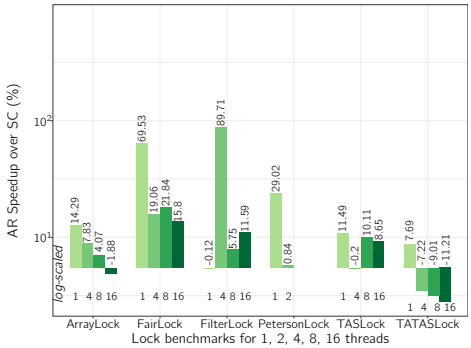


Experiment:

- N Threads
- 10M Lock/Unlock operations in a loop, no operation between Lock and Unlock
- 28 Cores, 2-socket system (Intel Xeon E5-2697 v3 @ 2.60 GHz)

from: S. Yang, S. Jeong, B. Min, Y. Kim, B. Burgstaller, J. Blieberger, *Design-space evaluation for non-blocking synchronization in Ada: lock elision of protected objects, concurrent objects, and low-level atomics*, Journal of System Architecture, Volume 110, 2020, 101764, ISSN 1383-7621, https://doi.org/10.1016/j.sysarc.2020.101764 .

Performance Gain ARM v8 through SC→AR-Relaxation



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- $\Rightarrow$ weak memory model: **Relaxed Memory Model**.
- Practical compromise between programmers' intuition and performance: **Release/Acquire Memory Model**

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- Freely accessible, open-source libraries are better!