Hardware Modelling

Design Flow: SVD – CFT – PPP – MTC
Strategy Implementation Validation

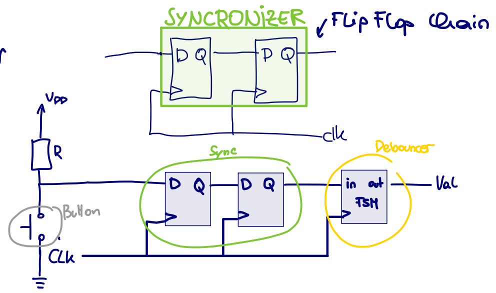
5% – 80% – 15% → 5% – 25% – 70%

Structural Developement: Systematic Approach, Hierarchial Structure

design: top – down ↓
verification: bottom – up ↑ (implementation)

Design Challenges: asynchronous inputs → synchronizer

debouncer → multiple inputs



metastability, switches for direction, reset button

Clk generation:

PLL : Phase Locked Loops

Delay causes: change of flow current (Wechsel strom)

pulse shape: threshold voltage, load capacitance

VHDL: pure (inertial) delay || pulse width degradation || single history delay channels || involution IDM

State Machine Design: for temporal order, Moore Machines

implementation
1 process method: @ rising_clk_edge
2/3 process method: sync + async Process

Design Entry: Reusability → reduces implementation | verification effort
→ finite partitioning, good documentation, use of packages, components, generics
→ templates, packages

Records: adding ports, registers, tracking signals during debug

Reset

Synthesis: Physically awareness, timing analysis, constraints, optimization, attributes,

(pins; path = cell + interconnect delay; possible delays; specify properties; timing adapted; fulfil constraints, power during routing)

Verification: validation, functional verification, formal verification (proof SAT) (LTL)

code coverage, design for testability