Exam

Advanced Digital Design

January 27, 2021

The working time is 90 minutes. The only allowed tools are writing utensils, a non-programmable pocket calculator and a ruler. Write your answers (including **explanatory statements**) with an ink pen or a ball-point pen (not in red, no pencil) and strike out everything, which should not be considered for grading. Only use the **front side of every page**, i.e., don't flip pages around and write on the backside! Enter your name, the code of your study and your student ID **at the beginning** of the exam in the table below.

Last Name:	First Name:
Code of Study:	Sudent ID:

Good luck!

Do not fill out the following table!

Task		Maximum Points	Achieved Points
	1	22	
	2	22	
	3	22	
	4	22	
	5	12	
Total		100	

Task 1: Hazards

Analyze the circuit given in Figure 1.

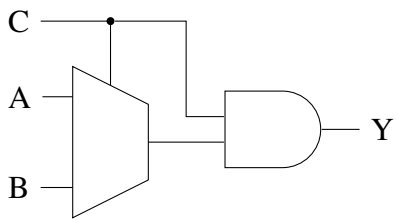


Figure 1: Circuit

a) In a first step, analyze the multiplexor alone, i.e., disregard the AND gate at the output. How can you construct it from AND gates, OR gates and inverters? Derive a sum-of-products implementation.

b) Identify all SIC hazards in the implementation you came up with, using any of the means presented in the lecture! Are there static hazards? Are there dynamic hazards? For both types, list all of them (along with their enabling and triggering conditions), and give an argument why your list is complete!

c) Can you eliminate the hazards through redundant terms? Explain how, or, why this is not possible!

d) Now consider the whole circuit, including the AND gate. List all dynamic SIC hazards along with their enabling and triggering conditions!

e) Can you eliminate these hazards through adding delay elements? Explain how, or, why this is not possible!

Task 2: Metastability

Assume you start in a new company, which designs dependable HW systems. Your first task is to improve a circuit built by a former employee, who was recently fired. The given circuit was designed for handing over data between two different clock domains.

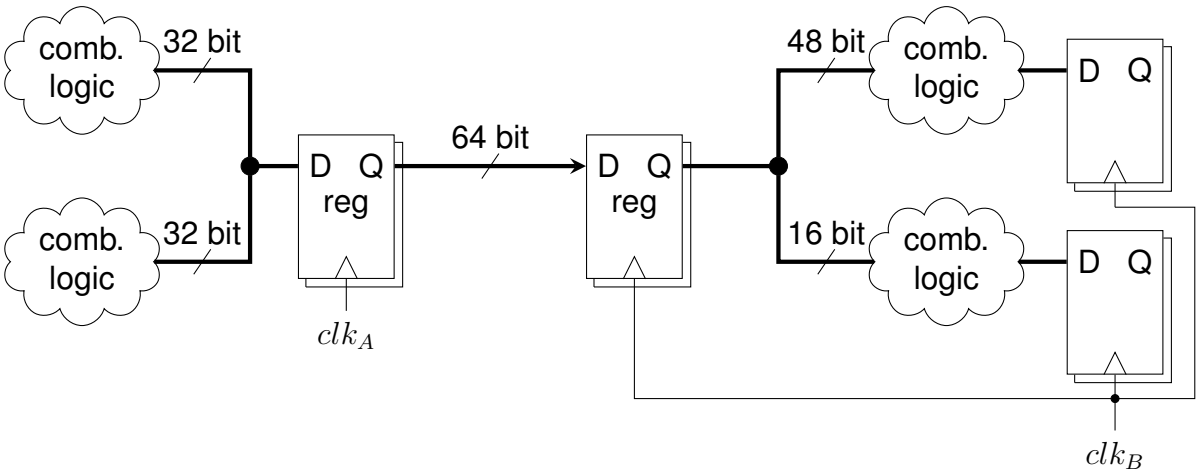


Figure 2: Clock Domain Crossing Circuit

Parameters:

- Clocks: $clk_A = 201MHz,\ clk_B = 250MHz$
- All registers: $t_{setup} = 0.2ns,\ t_{clk2output} = 0.5ns,\ \tau_c = 0.1ns,\ T_0 = 0.1ns$
- Each combinational cloud: $t_{comb} = 1ns$

The requirements of the customer are:

- Minimum data throughput: 2 Gbit/s
- On average a faulty data transfer must not happen more than once in 10 years
- Guarantee that no faulty data transfer occurs within the first 3 months

a) Can the circuit illustrated above meet these requirements? Which can be met? Explain why (or why not)?

b) Work out an idea for improving the circuit above! Which of the customer's requirements can be met with your circuit? Explain why (or why not)?

Task 3: QDI Function Block Design

Consider the 3-input 4-phase QDI dual-rail function block shown in Figure 3. $X.F$ denotes the false rail of the dual-rail signal X, while $X.T$ denotes the true rail.

a) Which logic function is implemented by this circuit?

b) What is the purpose of the $done$ signal?

c) Embed the function block in a WCHB pipeline. Draw one stage that feeds the function block and one stage at the output. Use the template shown in Figure 5 for that purpuse.

d) Implement an equivalent version of the circuit in Figure 3 using the DIMS design style!

e) How can an inverter be implemented using the DIMS design style?

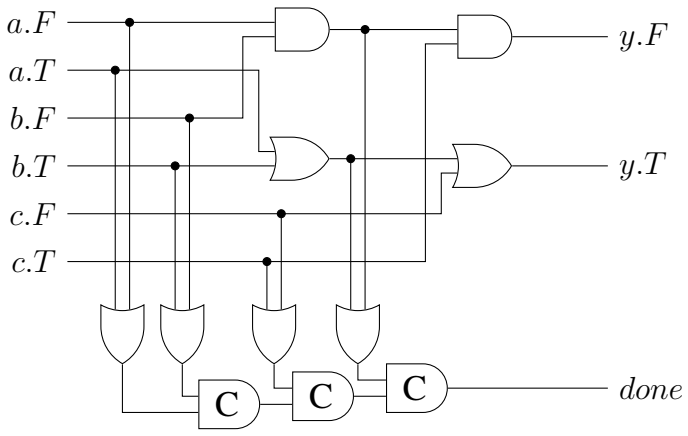


Figure 3: 4-phase QDI dual-rail function block

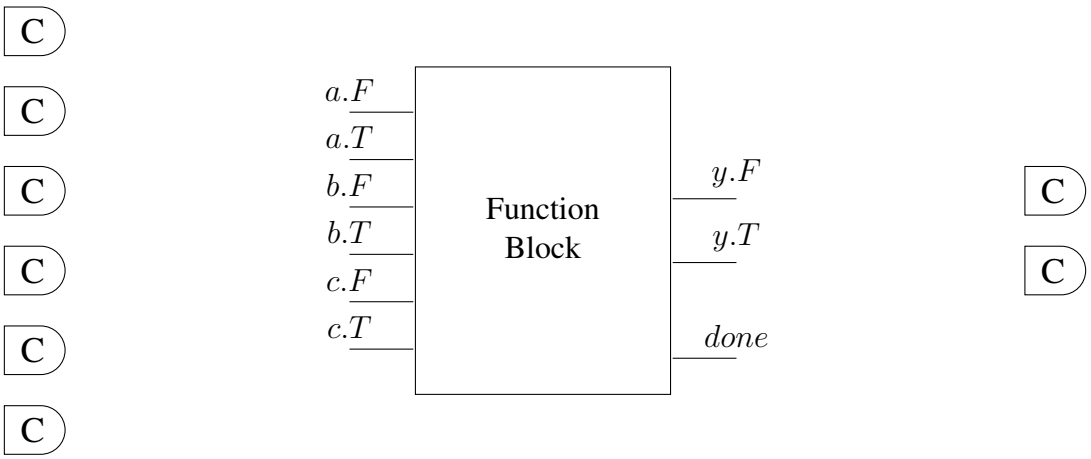


Figure 4: WCHB pipeline template

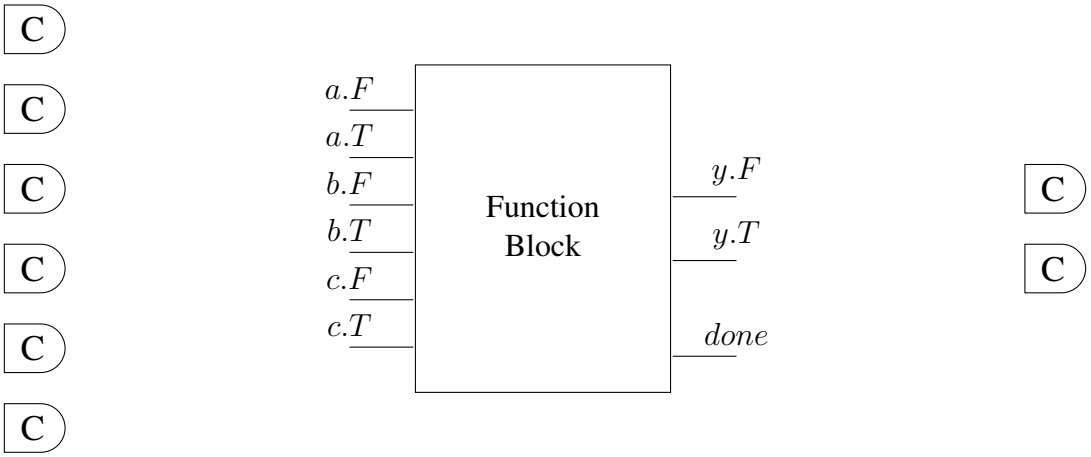


Figure 5: WCHB pipeline template (SPARE)

Task 4: STG-Synthesis

a) Draw an STG specifying the behavior of a 3-input C gate where one input is inverted (see Figure 6). Don't forget to also include a valid initial marking of the STG (i.e., the edges and/or places that contain tokens). Further assume a well-behaved environment, i.e., transitions on the inputs (a, b, c) only happen after a transition on the output (y).

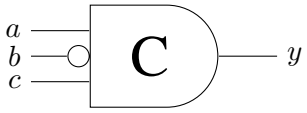
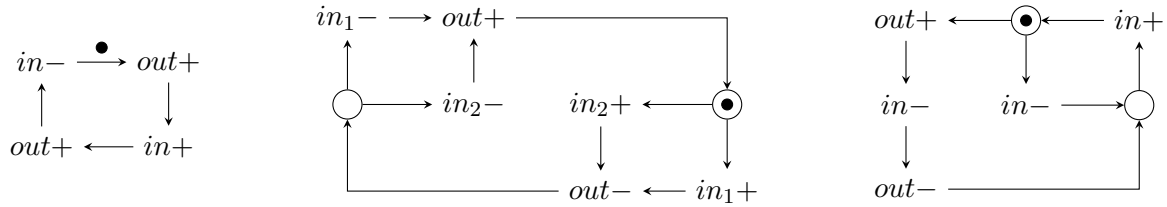


Figure 6: 3-input C gate with one inverted input

b) STGs must satisfy certain properties to be valid. These include liveness (i.e., deadlock-freeness), persistency and consistency (i.e., consistent state assignment). The three STGs shown in Figure 7 all violate one of these properties. Assign the property-violations to the STGs and explain how and why the respective STG violates the property.



STG (A) STG (B) STG (C)

Figure 7: Invalid STGs

c) Consider the STG and the state graph derived from it shown in Figures 8 and 9. The variables a and b are inputs while the variables x and y are outputs.

i) What is the variable order used for the state labels? Note that the last 4 digits of the state label correspond to the binary encoded state!

ii) Identify and mark all CSC conflicts in the state graph (use Figure 9).

iii) Resolve the CSC conflict by introducing an additional edge in the STG (i.e., by reducing its concurrency). Draw the resulting STG and show how this changes the state graph (use the template in Figure 10 for that purpose, use the free space above the stage graph to draw the STG).

iv) Resolve the CSC conflict by introducing a new internal state variable called csc into the STG. Draw the resulting STG and show how this changes the state graph (use the template in Figure 11 for that purpose, use the free space above the stage graph to draw the STG). Don't forget to also change the state labels (specify the new variable order you used)!

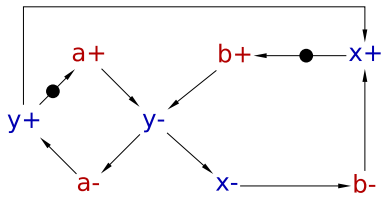


Figure 8: STG

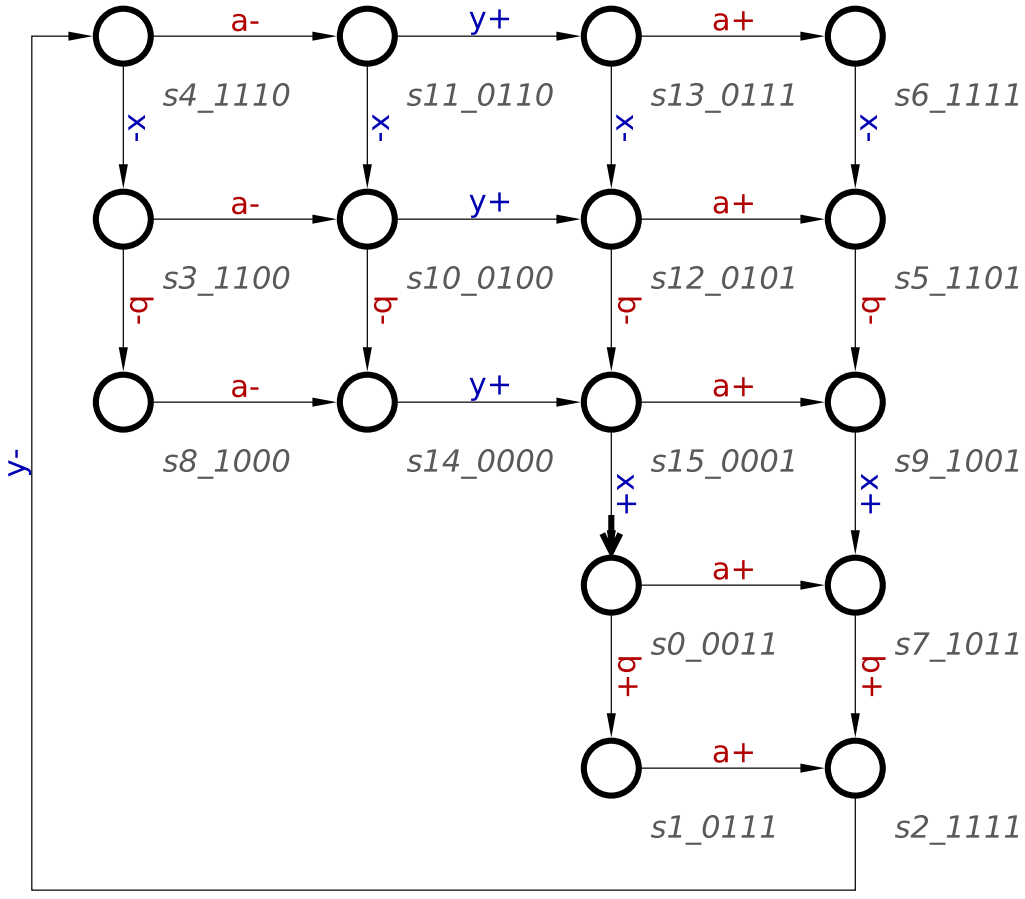


Figure 9: State Graph

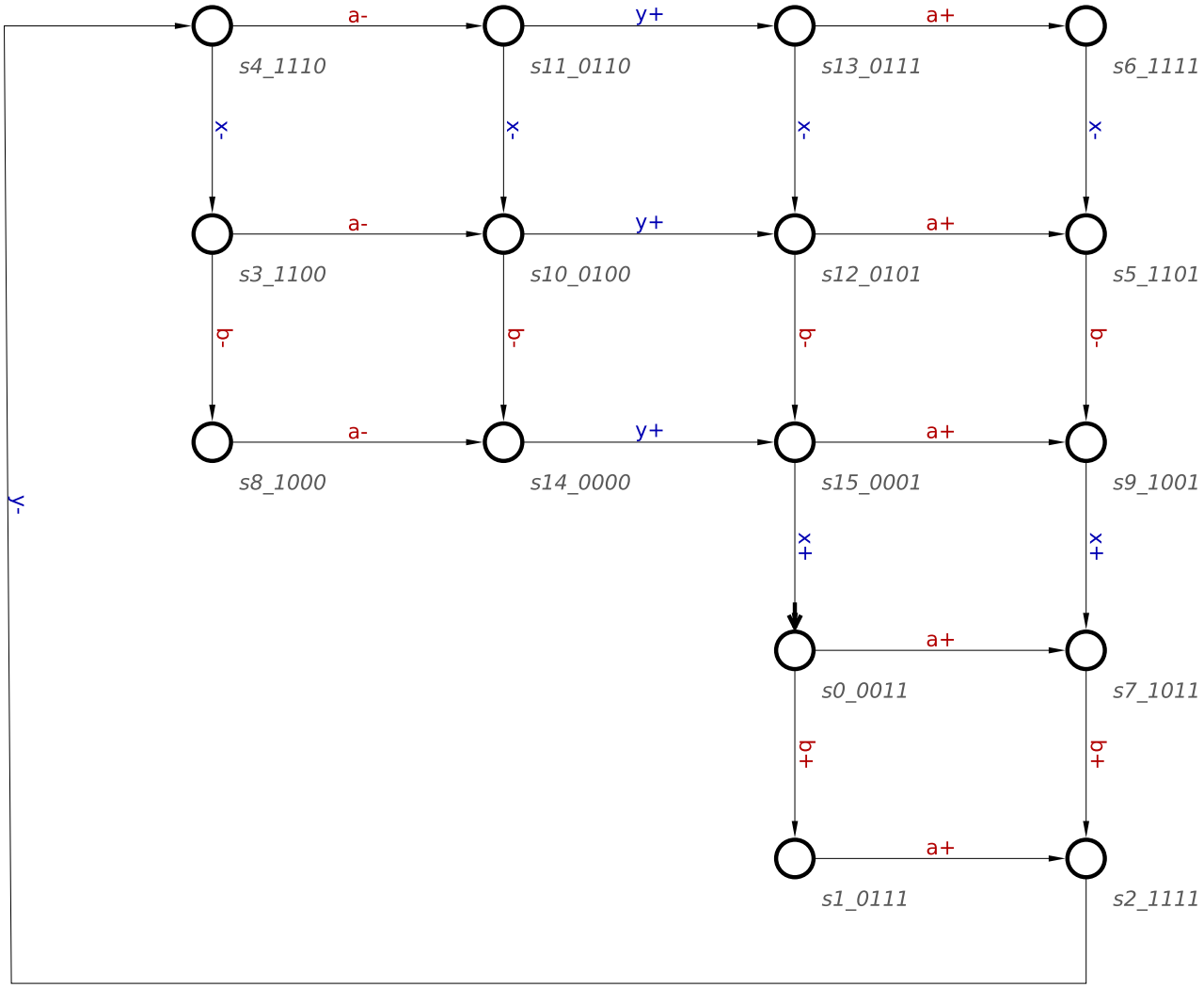


Figure 10: State Graph

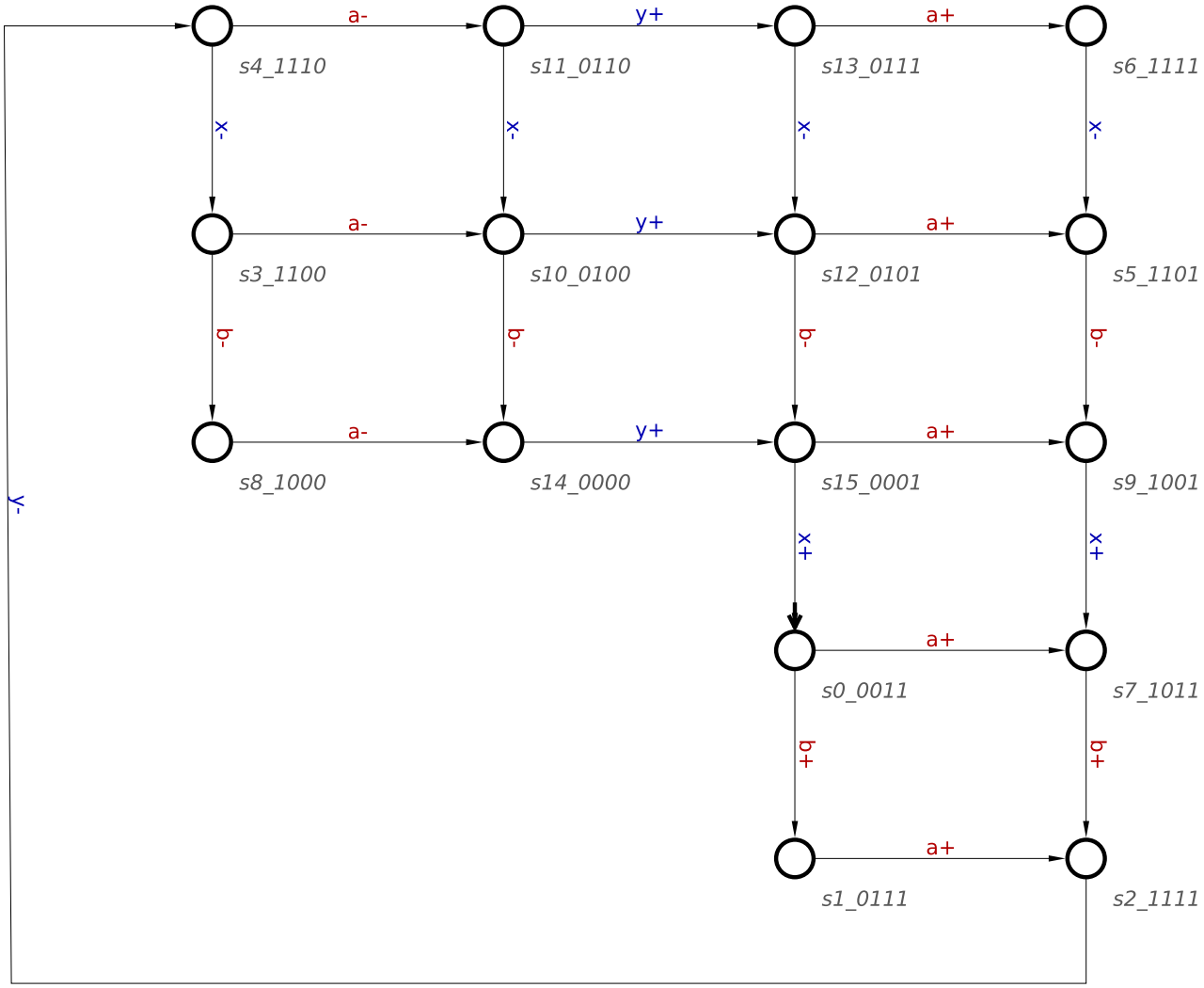


Figure 11: State Graph

Task 5: Pausible Clock

You have just been hired in a chip design company, and your boss tells you to look at a circuit for a pausible clock that your predecessor had designed before he got fired because he could not make the circuit work. The circuit diagram is shown in Figure 12.

Make the necessary corrections to the circuit (there should be 3). You can draw directly into the figure (No need to give explanations).

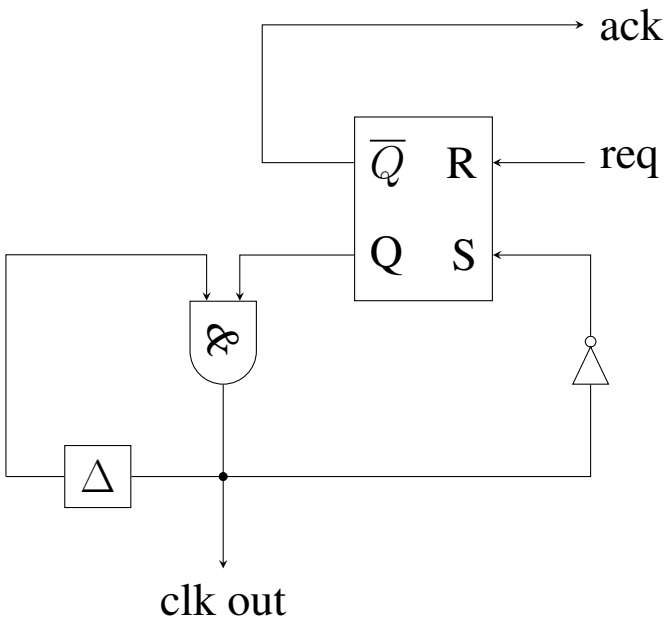


Figure 12: Erroneous pausible clock circuit