Informatics

Motivation

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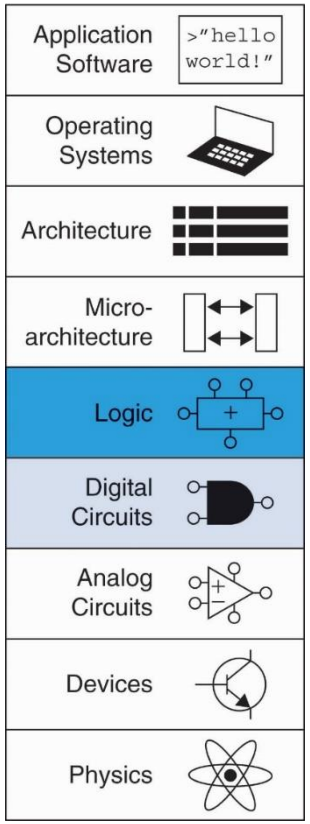
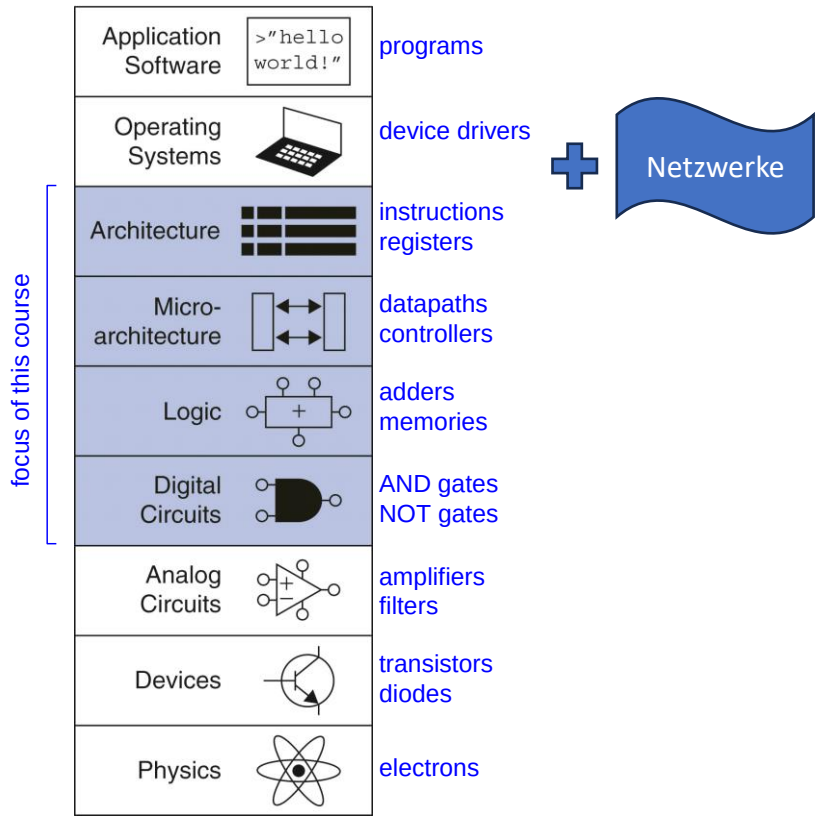
Content

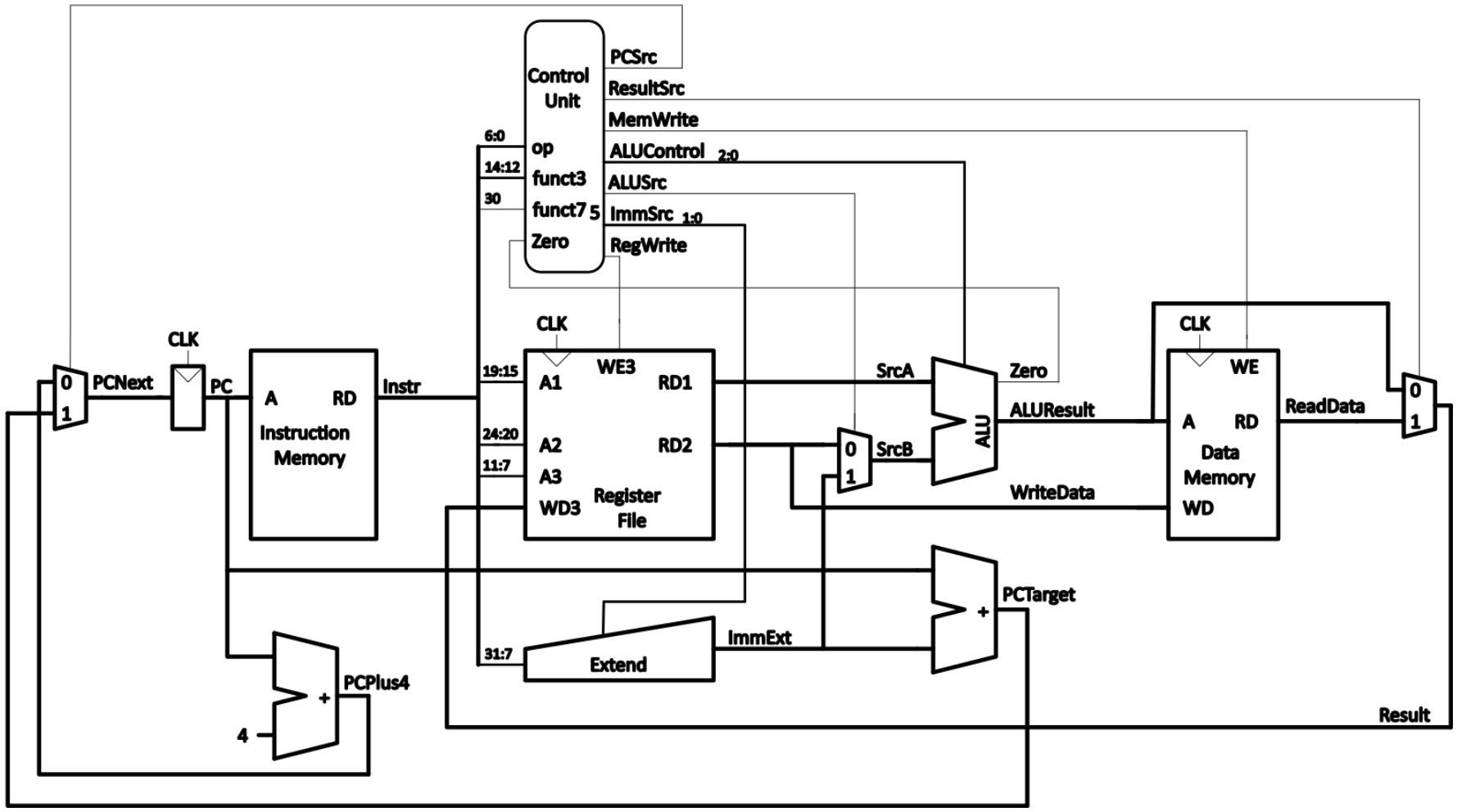
Grundzüge Digitale Systeme



Computersysteme



This is a Single-Cycle RISC-V Processor



RISC-V

RISC-V, offizielle Aussprache in Englisch: „risc-five“[1] [rɪsk faɪv], ist eine Befehlssatzarchitektur (engl. *instruction set architecture*, ISA), die sich auf das Designprinzip des Reduced Instruction Set Computers (RISC) stützt. Es ist ein offener Standard, welcher der freien BSD-Lizenz unterliegt. Das bedeutet, dass RISC-V nicht patentiert ist und frei verwendet werden darf. Somit ist es jedem erlaubt, RISC-V Mikroprozessoren zu entwerfen, herzustellen, weiterzuentwickeln und zu verkaufen (Open-Source-Hardware).[2] Zahlreiche Unternehmen bieten RISC-V-Hardware an oder haben diese angekündigt.

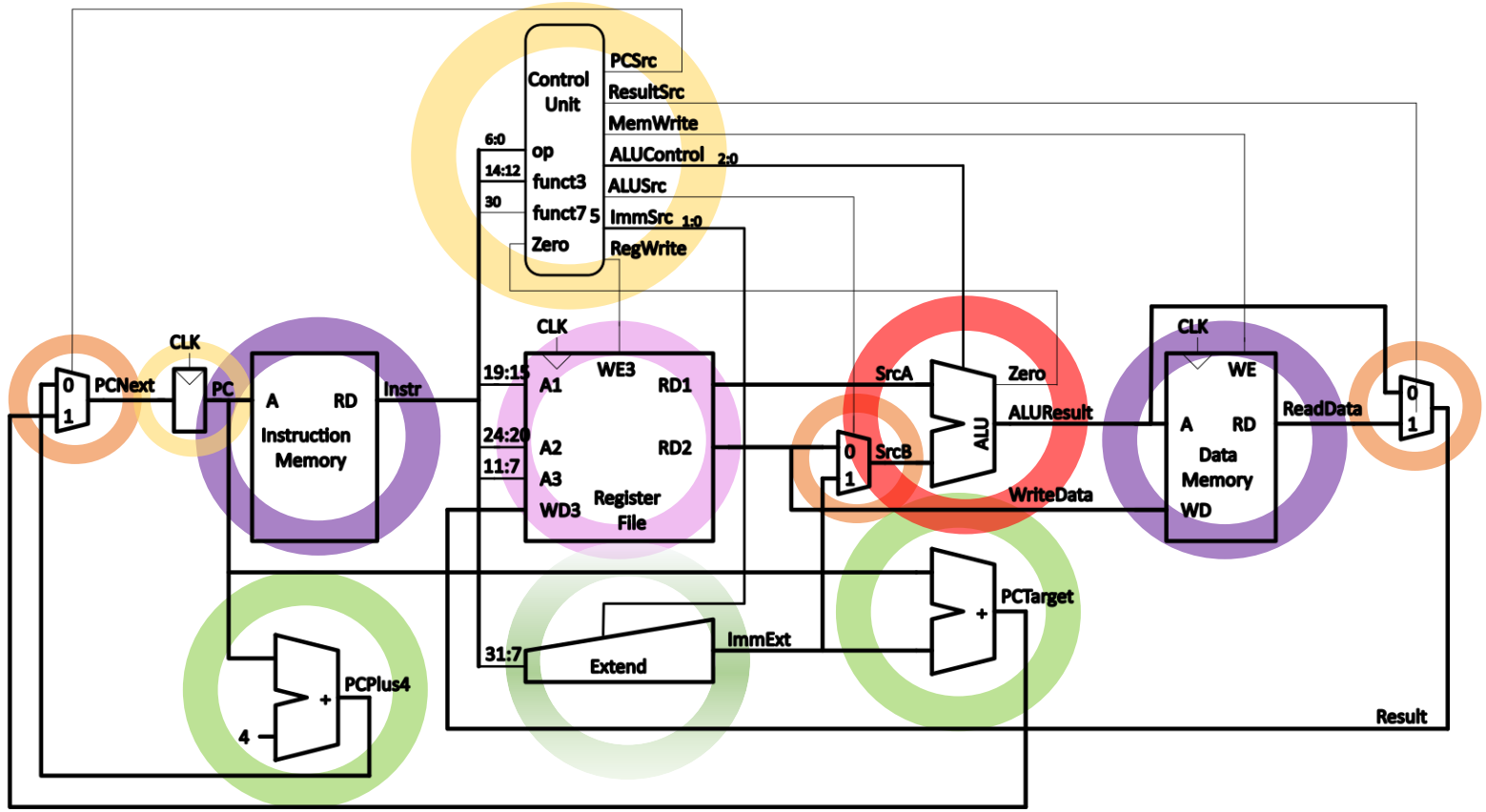
[https://de.wikipedia.org/wiki/RISC-V]

Arm Cortex-M (in älterer Schreibweise **ARM Cortex-M**) ist eine Familie von IP-Cores primär für 32-Bit-Mikrocontroller, die vom Unternehmen ARM entwickelt wird und an verschiedene Hersteller lizenziert wird. Der Kern stellt eine Reduced Instruction Set Computer (RISC) dar, ist ein Teil der ARMv6- bzw. Armv7-Architektur[1] und unterteilt sich in aufsteigender Komplexität in die Einheiten Cortex-M0,[2] Cortex-M0+,[3] Cortex-M1,[4] Cortex-M3,[5] Cortex-M4[6], Cortex-M7 und die auf der Armv8-Architektur basierenden Cortex-M23,[7] und Cortex-M33.[8]

[https://de.wikipedia.org/wiki/Arm_Cortex-M]

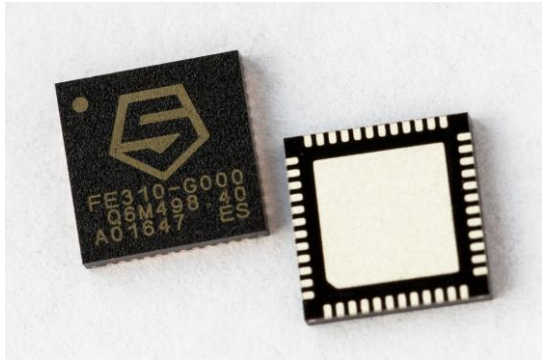
Components

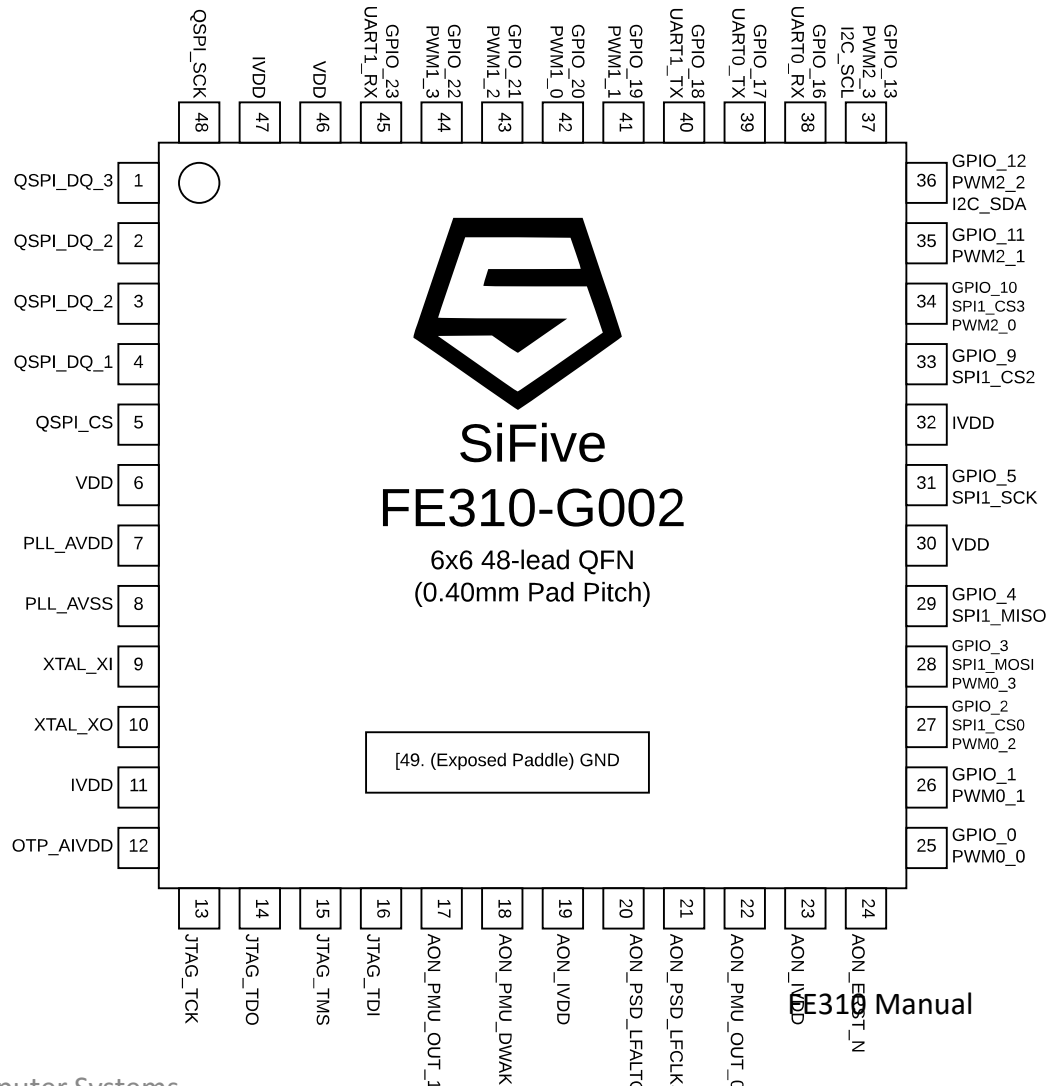
- Mutliplexer
- Adder
- Sequential Circuit (Schaltwerk)
- Memory
  - SRAM
  - DRAM
- ALU



FE310 Pinout

- 48-pin QFN (quad flat pack, no leads)
  - Hard to hand solder
- Pins:
  - 12 power (GND pad on back)
  - 19 GPIO
  - 4 JTAG programming
  - 6 QSPI Flash code link
  - 2 clock crystals
  - 6 control

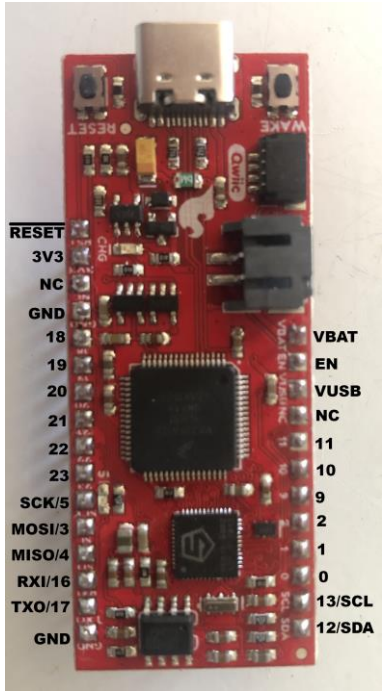




FE310 Manual

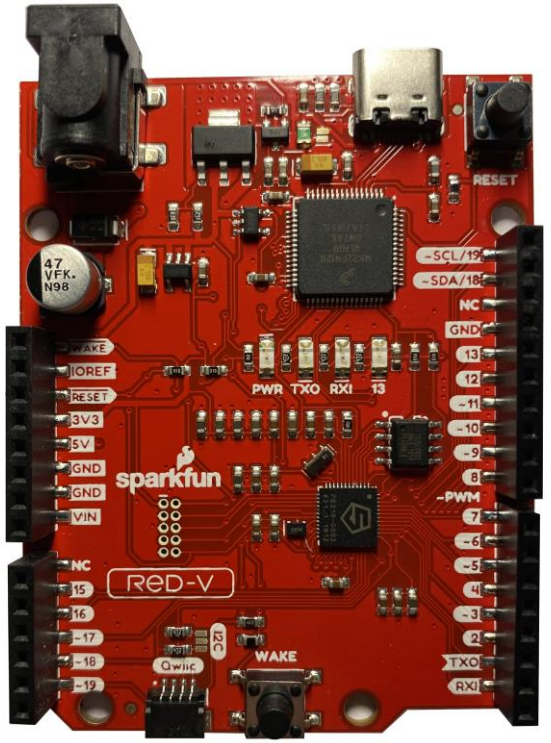
Boards

SparkFun RED-V Thing Plus



$30
Fits breadboard (2.3x0.9”)
Requires soldering
header pins

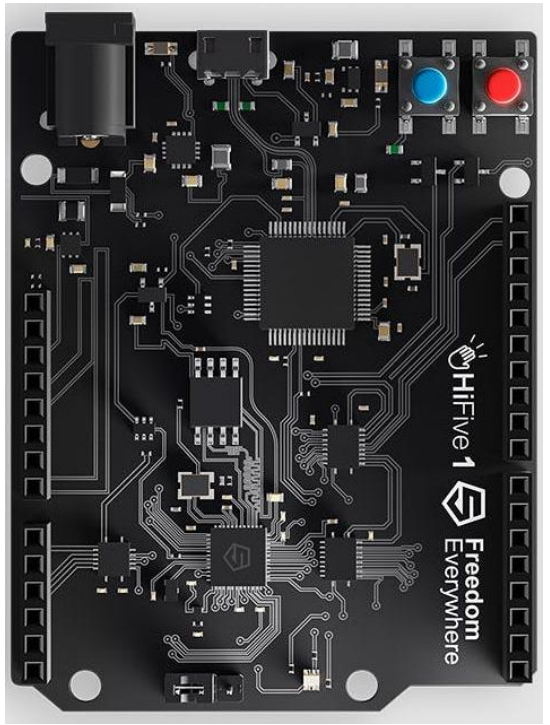
SparkFun RED-V RedBoard



sparkfun.com

$40
Headers soldered
Nonstandard pin labels

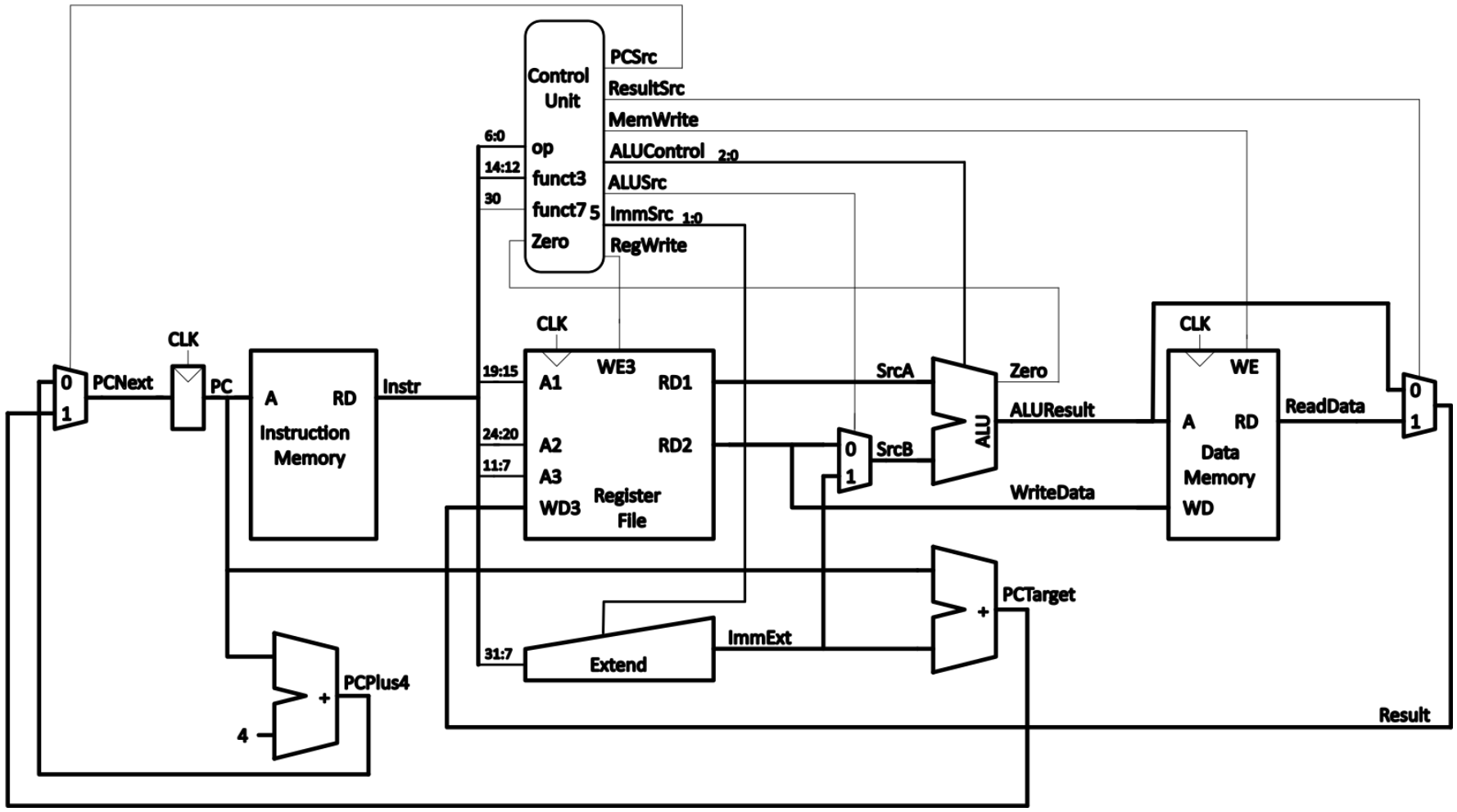
HiFive 1



sifive.com

$60
WiFi & Bluetooth

This is a Single-Cycle RISC-V Processor

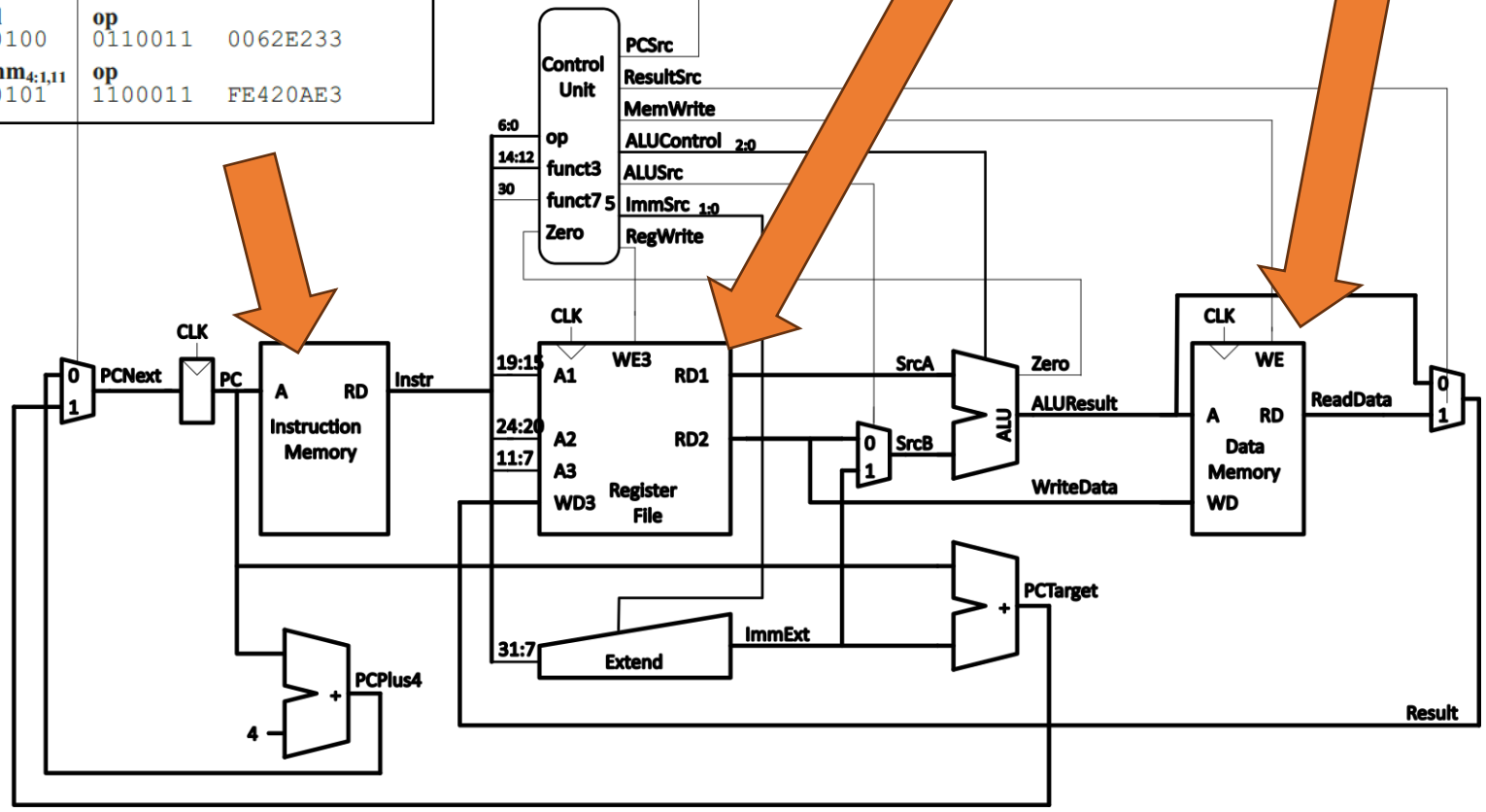


Single-Cycle Datapath

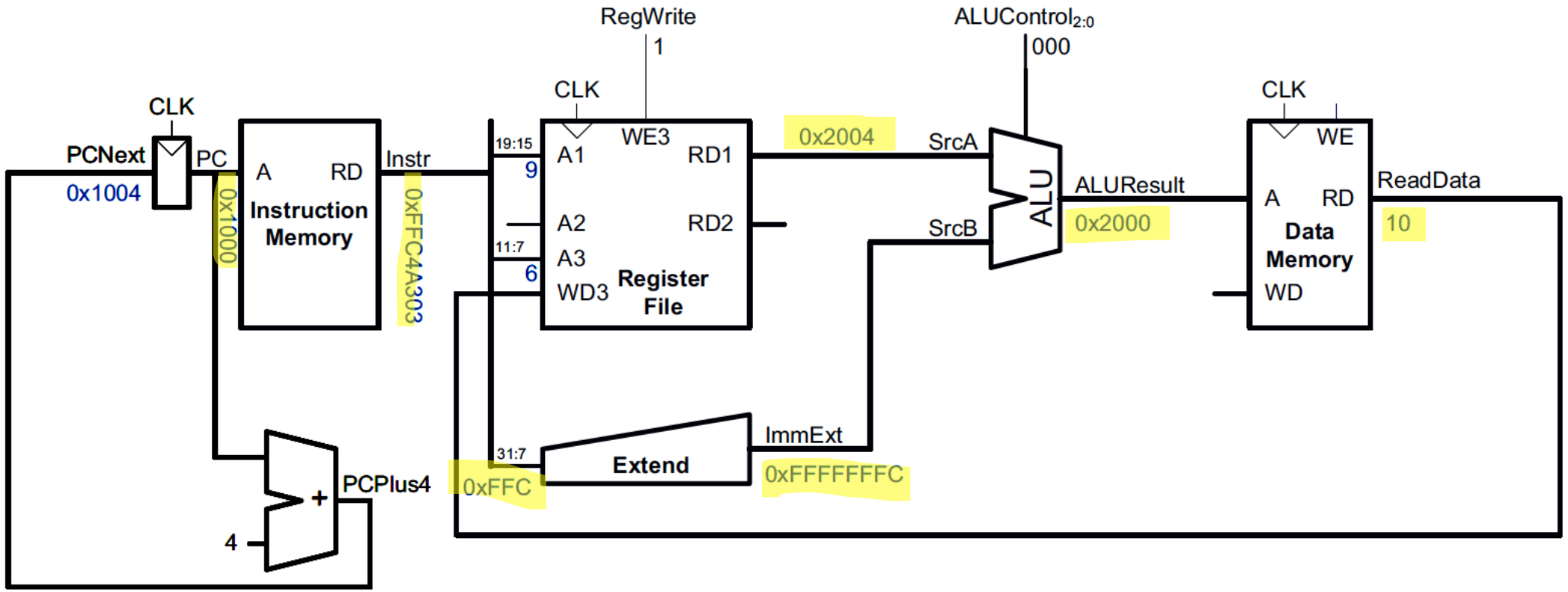
Address	Instruction	Type	Fields					Machine Language
			$imm_{11:0}$	rs1	f3	rd	op	
0x1000	L7: lw x6, -4(x9)	I	111111111100	01001	010	00110	0000011	FFC4A303
			$imm_{11:5}$ rs2	rs1	f3	$imm_{4:0}$	op	
0x1004	sw x6, 8(x9)	S	0000000 00110	01001	010	01000	0100011	0064A423
			funct7 rs2	rs1	f3	rd	op	
0x1008	or x4, x5, x6	R	0000000 00110	00101	110	00100	0110011	0062E233
			$imm_{12,10:5}$ rs2	rs1	f3	$imm_{4:1,11}$	op	
0x100C	beq x4, x4, L7	B	1111111 00100	00100	000	10101	1100011	FE420AE3

@0x200 = 10d

x9 = 0x204

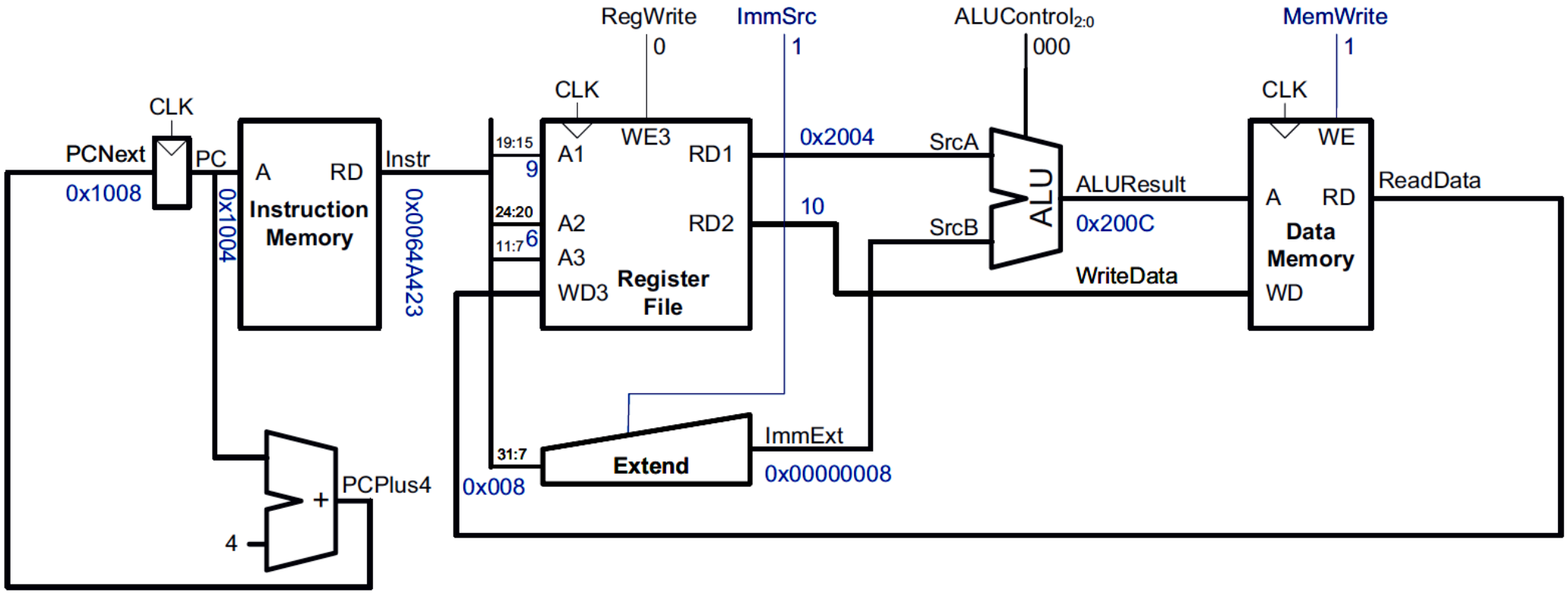


lw instruction, 0xFFC4A303



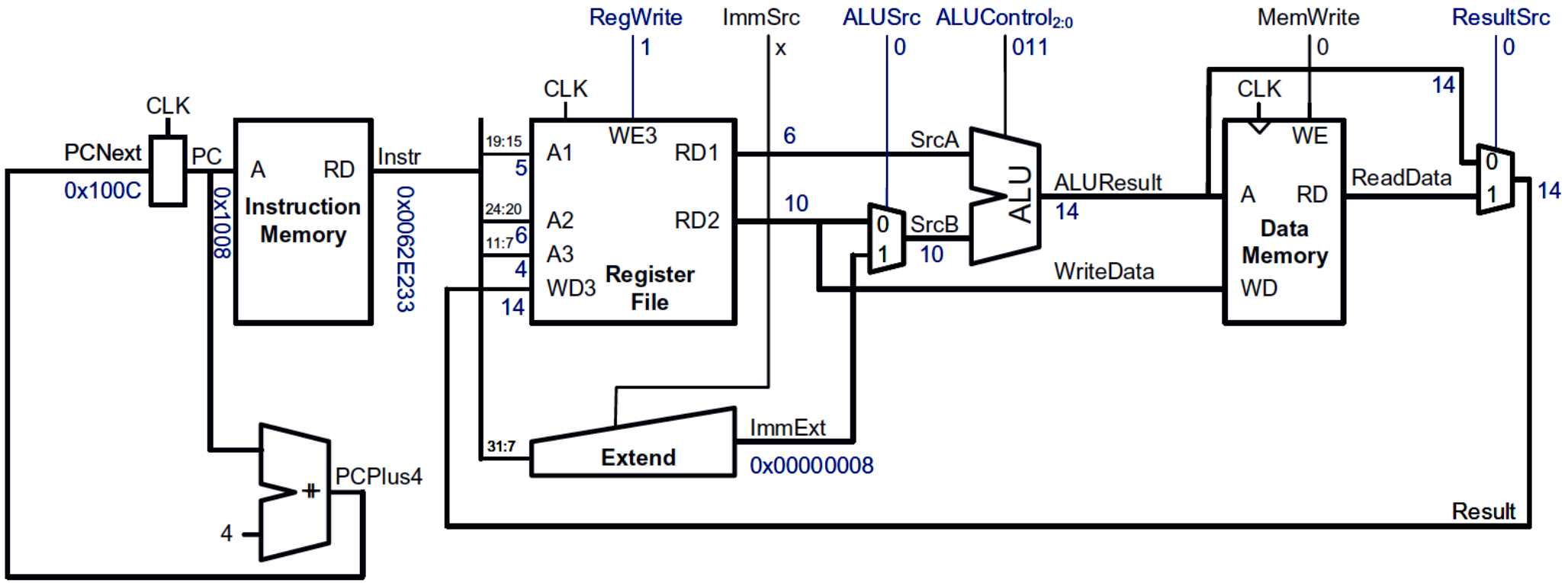
Address	Instruction	Type	Fields					Machine Language
			$imm_{11:0}$	rs1	f3	rd	op	
0x1000	L7: lw x6, -4(x9)	I	111111111100	01001	010	00110	0000011	FFC4A303

sw instruction, 0x0064A423



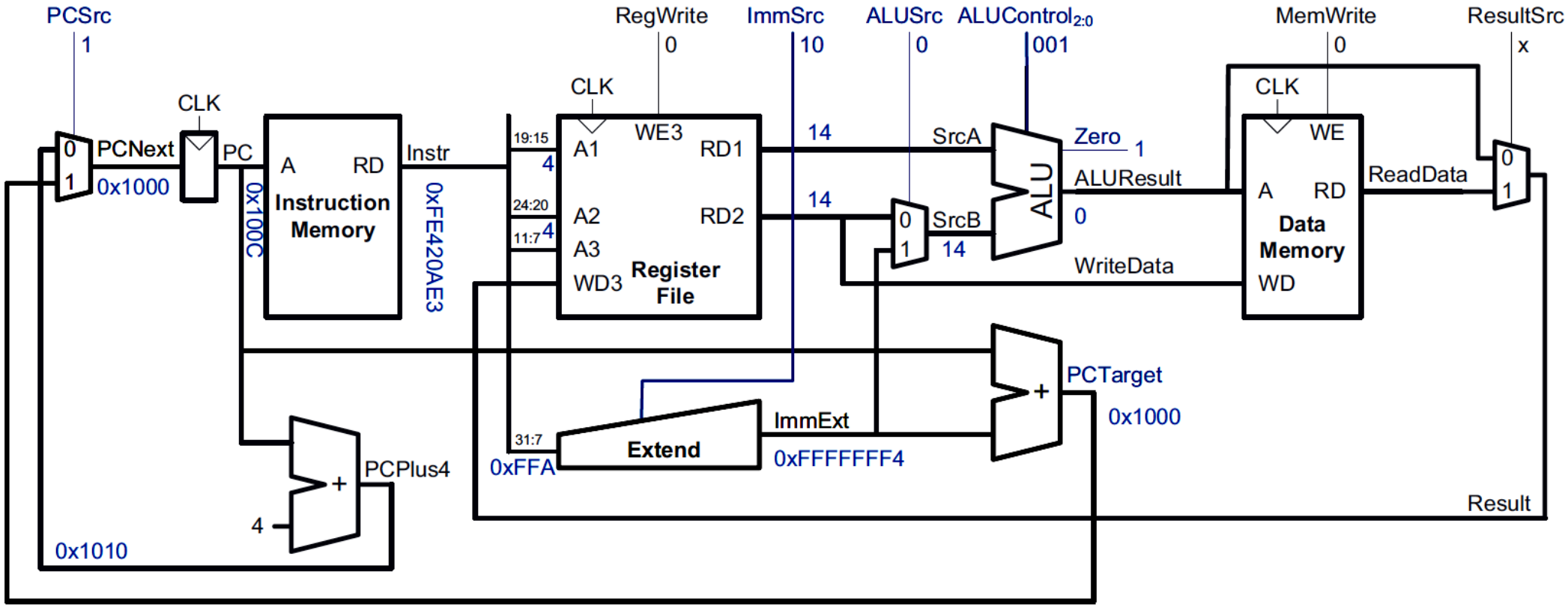
Address	Instruction	Type	Fields					Machine Language
			$imm_{11:5}$	rs2	rs1	f3	$imm_{4:0}$	op	
0x1004	sw x6, 8(x9)	S	0000000	00110	01001	010	01000	0100011	0064A423

or instruction, 0x0062E233



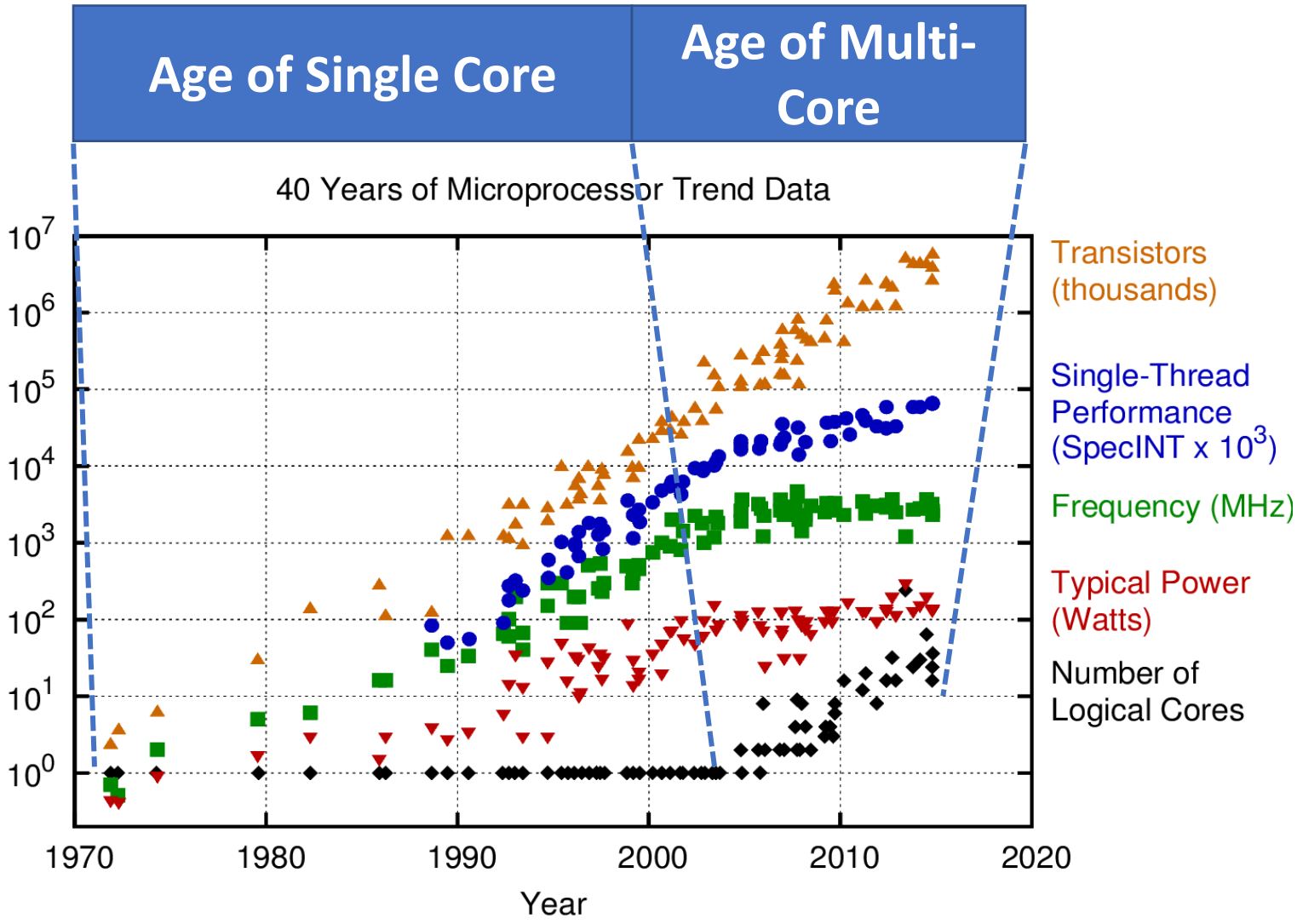
Address	Instruction	Type	Fields					Machine Language
			funct7	rs2	rs1	f3	rd	op	
0x1008	or x4, x5, x6	R	0000000	00110	00101	110	00100	0110011	0062E233

beq instruction, 0xFE420AE3



Address	Instruction	Type	Fields						Machine Language
			$imm_{12,10:5}$	rs2	rs1	f3	$imm_{4:1,11}$	op	
0x100C	beq x4, x4, L7	B	1111111	00100	00100	000	10101	1100011	FE420AE3

Computing Trends: Where are we?



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2015 by K. Rupp

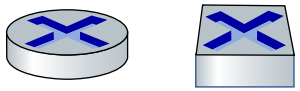
So why learn about Computing Systems

- Any class of system (from embedded systems to servers) now integrates a wide range of dedicated processing:
  - General-purpose: Single/Multi-cores processors (with special instructions: RISC-V)
  - GPUs
  - Accelerators (e.g., so called NPUs/TPUs for machine learning)
  - Even FGPAs (programmable hardware)
- Software must exploit dedicated processing to meet performance/energy targets

Developers need a basic understanding from the low-level digital hardware up to computer architectures as well as of the memory system and interconnect organization.

The Internet: a “nuts and bolts” view

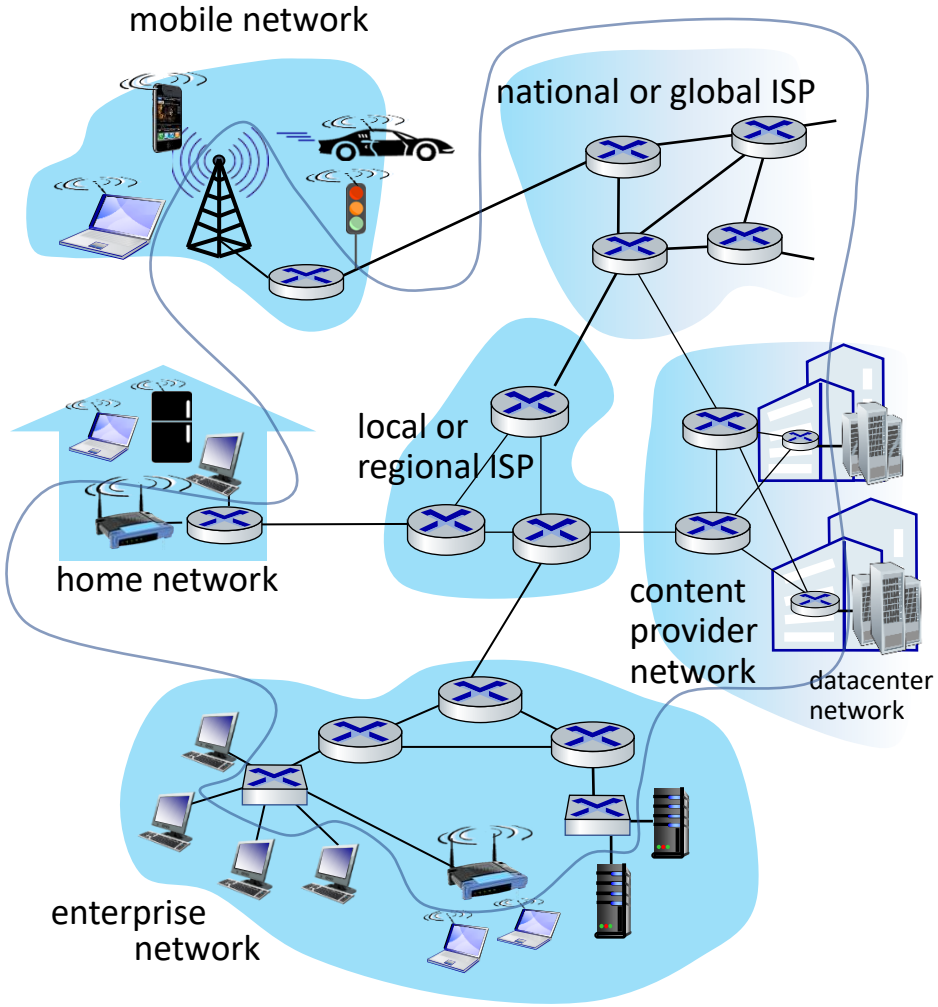
Billions of **devices** are connected to the Internet



Packet switches forward packets (chunks of data)

Communication Links allow transmitting data

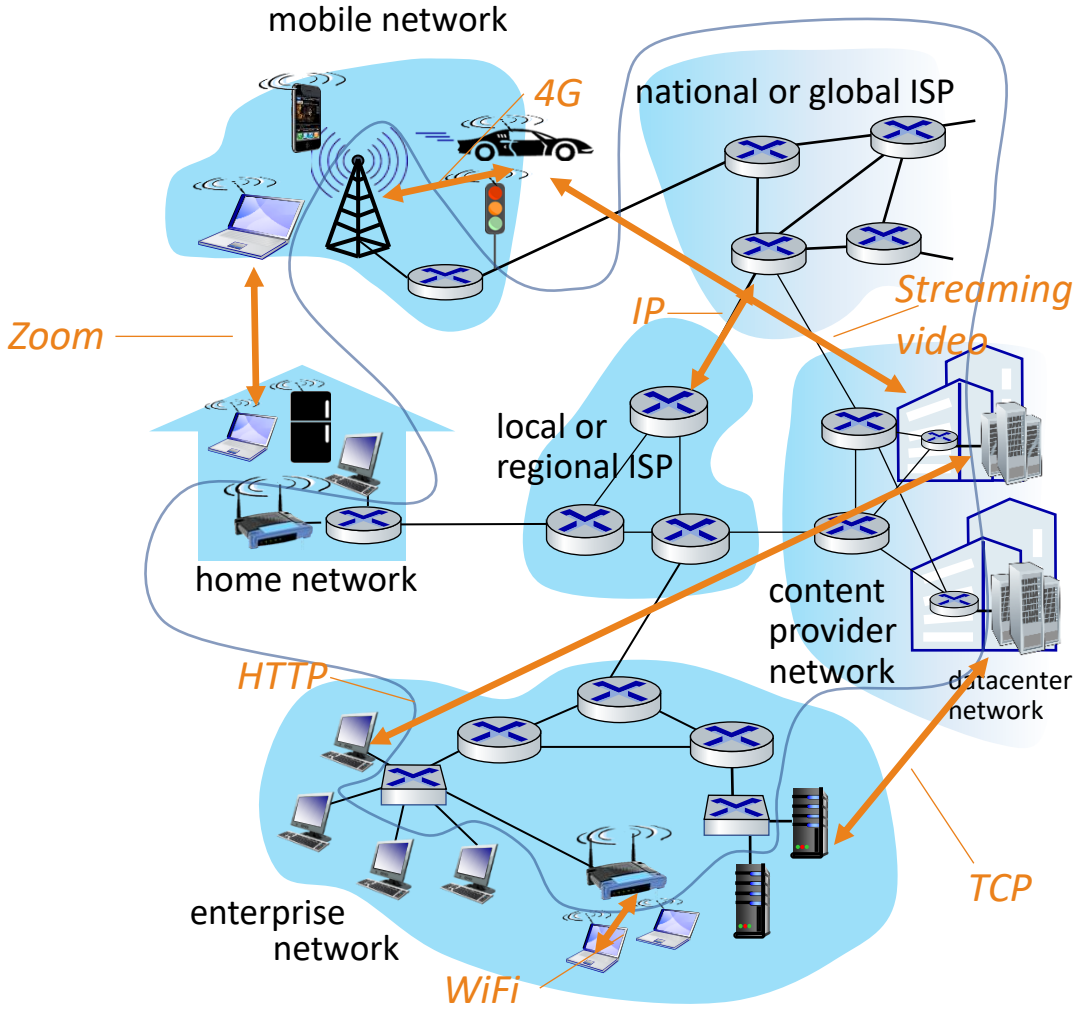
Networks are a collection of devices, packet switches and links (managed by an organization)



Kurose, James F., and Keith W. Ross. "Computer networking: A top-down approach"

The Internet: a “nuts and bolts” view

- The **Internet** is a **“network of networks”**
  - Interconnected ISPs
- Protocols are everywhere
  - Sending and receiving messages
  - For example: HTTP, video streaming, TCP, IP, Ethernet, …
- Internet Standards
  - RFC: Request for Comments
  - IETF: Internet Engineering Task Force



Kurose, James F., and Keith W. Ross. "Computer networking: A top-down approach"

Recap

- How a processor works
- How we deal with parallelism
- How do we interconnect systems
- How does the internet work
  - or at least some of the protocols

- You must work hard on your exercises
- You must write at least two exam

- We will make the lecture as exciting as possible

See you on Thursday