

Verification of Programs and Systems

Georg Weissenbacher

<https://www.forsyte.at>

for(sy)te, 
Formal Methods
in Systems Engineering

Bugs in the news ...



Toyota Prius

(New York Times, Feb. 12, 2014)

Toyota Motor is recalling all of the 1.9 million newest-generation Prius vehicles it has sold worldwide because of a programming error ...

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Heathrow Airport

(The Guardian, December 2014)

An unprecedented systems failure was responsible for the air traffic control chaos [...] “In this instance a transition between the two states caused a failure in the system which has not been seen before,” ...

Heathrow
Making every journey better

What goes up ...



Lufthansa Airbus A321

(Spiegel, March 20, 2015)

Beinahe wäre ein Airbus A321 der Lufthansa mit 109 Passagieren auf dem Flug von Bilbao nach München abgestürzt – irregeleitete Bordcomputer hatten die Kontrolle übernommen.

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Boeing 787 Dreamliner

(The Guardian, May 2015)

The US air safety authority has issued a warning and maintenance order over a software bug that causes a complete electric shutdown of Boeing's 787 ...



Some hardware bugs ...



Meltdown and Spectre

(New York Times, January 2018)

Called Meltdown, the first and most urgent flaw affects nearly all microprocessors by Intel. The second, Spectre, affects most other chips ...

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Rowhammer Bug

(InfoWorld, March 9, 2015)

...with certain varieties of DRAM an attacker can create privilege escalations by simply repeatedly accessing a given row of memory.







Toyota's killer firmware: Bad design and its consequences

Michael Dunn - October 28, 2013

[126 Comments](#)

Quelle: www.edn.com

- Oklahoma court ruled against Toyota in case of unintended acceleration that led to death
- Expert witness found numerous bugs in software (including bugs that can cause unintended acceleration), founds source code of “unreasonable quality”

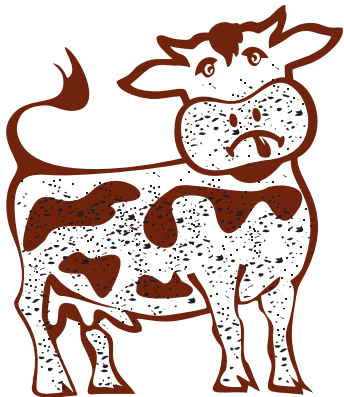
RISK ASSESSMENT —

“Most serious” Linux privilege-escalation bug ever is under active exploit (updated)

Lurking in the kernel for nine years, flaw gives untrusted users unfettered root access.

DAN GOODIN - 10/20/2016, 10:20 PM





DIRTY COW

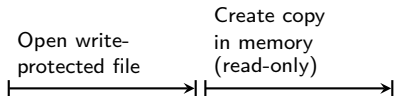
↪ "copy on write"

(CVE-2016-5195, published October 2016)

Anatomy of “Dirty Copy-On-Write” Attack

Goal: Write to protected systems file

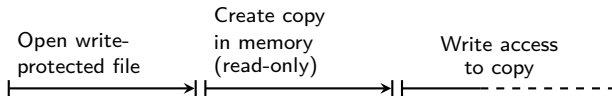
Copy-On-Write (COW) Upon write attempt, system creates copy of protected memory area



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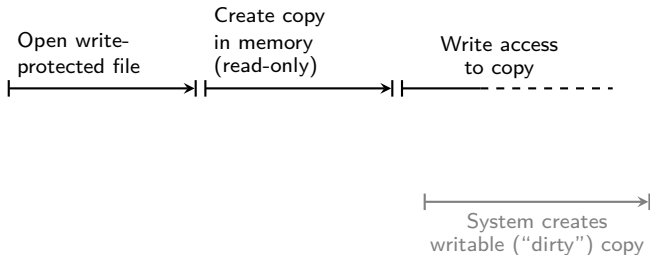
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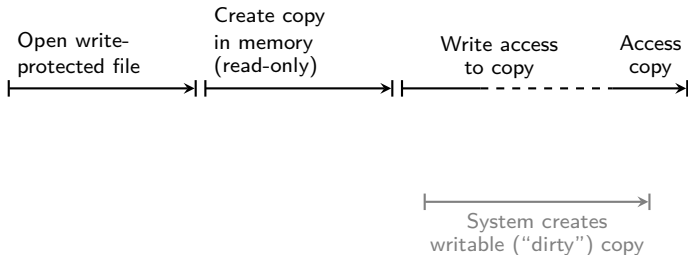
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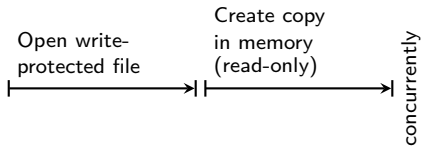
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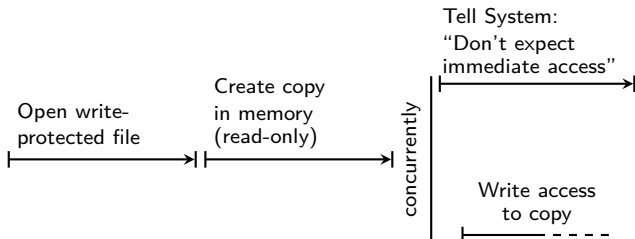
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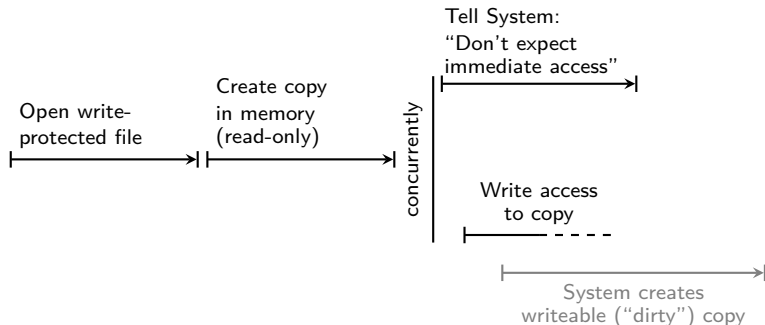
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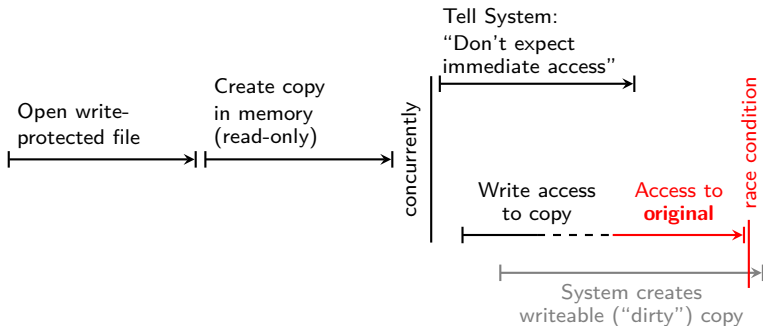
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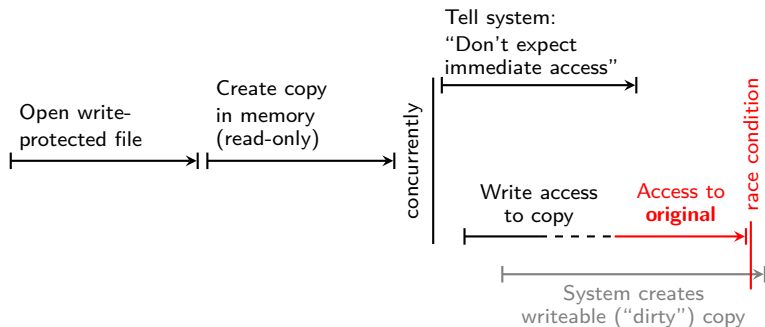
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Anatomy of “Dirty Copy-On-Write” Attack



Race Condition rarely happens

- *Testing* isn't particularly effective
- Systematic search (of schedules) is required

Another security bug ...

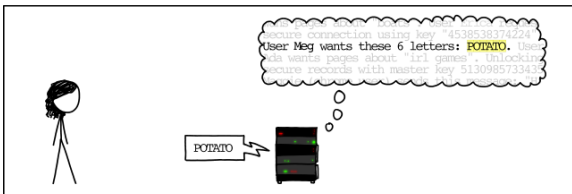


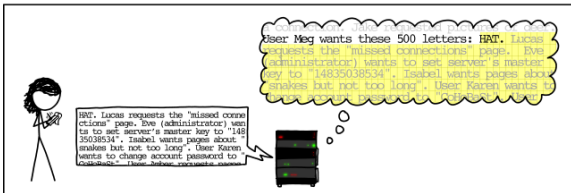
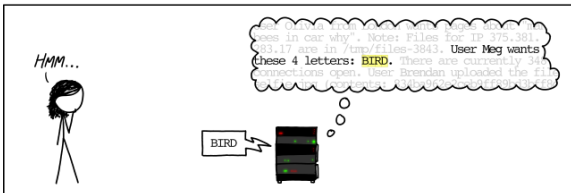
Heartbleed Bug

(CNN, April 9, 2014)

A major online security vulnerability dubbed “Heartbleed” could put your personal information at risk, including passwords, credit card information and e-mails.

HOW THE HEARTBLEED BUG WORKS:





Can you see it?

```
typedef struct {
    char* data;
    unsigned int len;
} ssl_buffer;

typedef struct {
    ssl_buffer buffer;
} SSL;

int tls1_process_heartbeat(SSL *s)
{
    char *p=s->buffer.data,*pl;

    unsigned short hbtype;
    unsigned int payload;
    unsigned int padding = 16;

    hbtype = *p++;
    n2s(p, payload);
    pl = p;
```

```
if (hbtype == TLS1_HB_REQUEST)
{
    unsigned char *buffer, *bp;
    int r;

    buffer = malloc(1 + 2 +
                    payload +
                    padding);

    bp = buffer;
    *bp++ = TLS1_HB_RESPONSE;
    s2n(payload, bp);
    memcpy(bp, pl, payload);
    bp += payload;
    RAND_pseudo_bytes(bp, padding);

    r = ssl3_write_bytes
        (s,TLS1_RT_HEARTBEAT,
         buffer,
         3 + payload + padding);
    free(buffer);
    if (r < 0)
        return r;
}
```


Let's use a tool to find the bug! (Try this at home)

- C Bounded Model Checker (CBMC):
<https://www.cprover.org/cbmc>
- Install command line tool
 - On Ubuntu: `sudo apt install cbmc (version > 5.10):`

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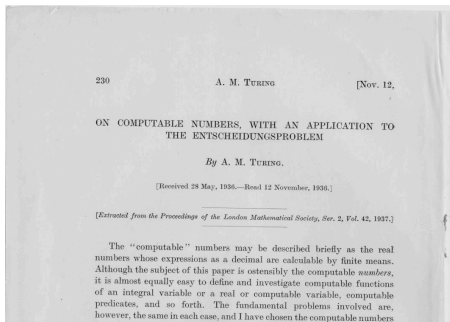
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- Run: `cbmc --pointer-check heartbleed.c`
- Output:
** Results:
<builtin-library-malloc> function malloc
[malloc.assertion.1] line 25 max allocation size exceeded: **SUCCESS**

src/heartbleed.c function tls1_process_heartbeat
[tls1_process_heartbeat.precondition_instance.1] line 54 memcpy
src/dst overlap: **SUCCESS**
[tls1_process_heartbeat.precondition_instance.2] line 54 memcpy
source region readable: **FAILURE**
[tls1_process_heartbeat.precondition_instance.3] line 54 memcpy
destination region writeable: **SUCCESS**

Can we always find bugs automatically?



Alan Turing (1912–1954)

Turing's Halting Problem

Turing's Halting Problem (1936)

Given a description of a program, decide whether the program finishes running or continues to run forever.

(undecidable)

Turing's Halting Problem

Proof ingredients:

- Program can be encoded as string
- Program operations can be simulated by Turing machine
- Diagonalization

Turing's Halting Problem (Proof Sketch)

Assume h is a computable function

$$h(i, x) = \begin{cases} 1 & \text{if program } i \text{ halts on input } x \\ 0 & \text{otherwise} \end{cases}$$

$$g(i) = \begin{cases} 0 & \text{if } h(i, i) = 0 \\ \perp & \text{otherwise} \end{cases}$$

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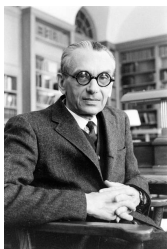
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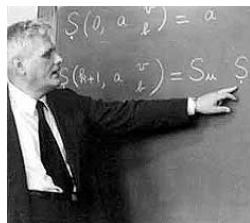
- $g(e) = h(e, e) = 0$. But e halts on input e , thus $h(e, e) = 1$
- $g(e) = \perp$ and $h(e, e) \neq 0$. But e doesn't halt, so $h(e, e) = 0$

Can we always find bugs automatically?



Kurt Gödel, 1931:
*Über formal entscheidbare Sätze
der Principia Mathematica und
verwandter Systeme*

Alonzo Church, 1936:
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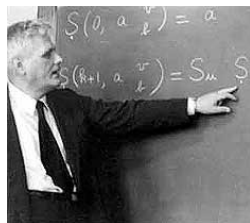


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Mission impossible?

What can be done?

“Software pioneers” in WW2



Alan Turing



Herman Goldstine
J. Robert Oppenheimer
John von Neumann

1115
" ECP

Report on the mathematical ...

PLANNING AND CODING OF PROBLEMS
FOR AN
ELECTRONIC COMPUTING INSTRUMENT

BY

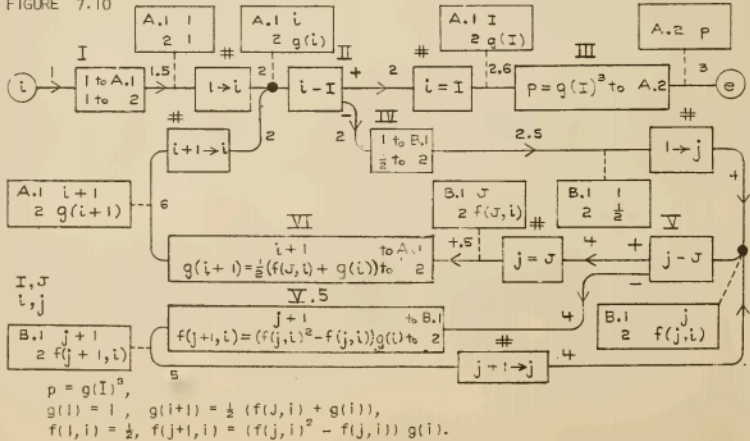
Herman H. Goldstine

John von Neumann

Report on the Mathematical and Logical aspects of an
Electronic Computing Instrument

Part II, Volume 1-3

FIGURE 7.10



An assertion box never requires that any specific calculations be made, it indicates only that certain relations are automatically fulfilled whenever C gets to the region which it occupies.

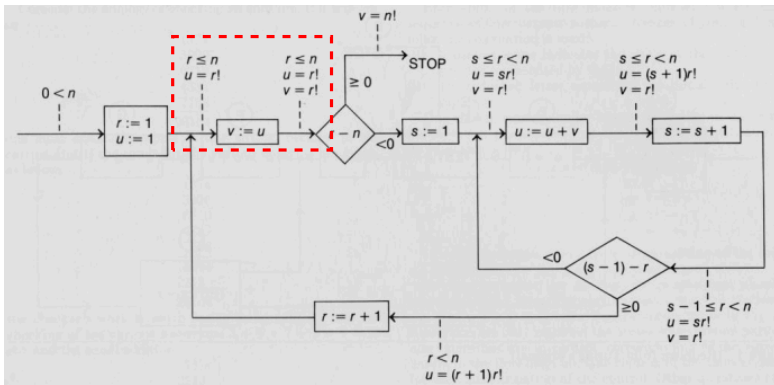
Turing didn't give up either

Friday, 24th June.

Checking a large routine. by Dr. A. Turing.

How can one check a routine in the sense of making sure that it is right?

In order that the man who checks may not have too difficult a task the programmer should make a number of definite assertions which can be checked individually, and from which the correctness of the whole programme easily follows.



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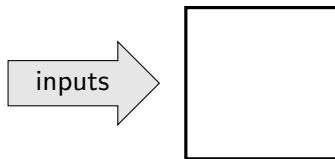
Questionnaire:

- Who of you writes programs?
- Who knows what assertions are?
- Who uses assertions?

Testing: The State-of-the-Art of Verification

How do we know Assertions hold?

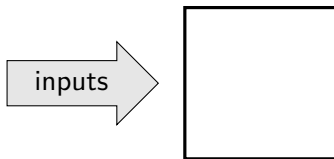
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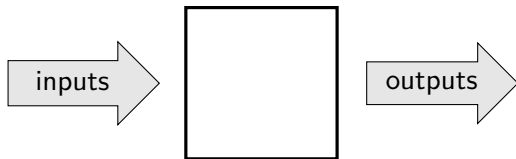
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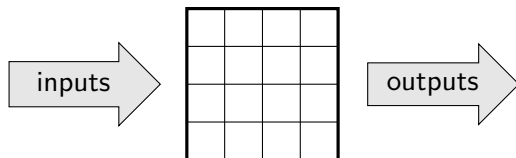
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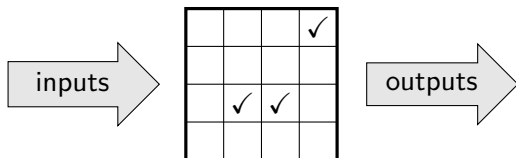
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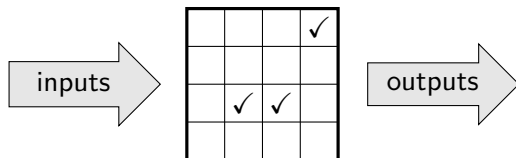
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Time for another questionnaire:

- Who of you tests *systematically*?
- Which coverage metrics do you know?

What are we even testing?

Does the program behave as specified?

- Specification
 - Required ingredients: Formalism, Assertion Language
- Program
 - Required ingredients: Language semantics

Assertions and Program Semantics



Robert W. Floyd

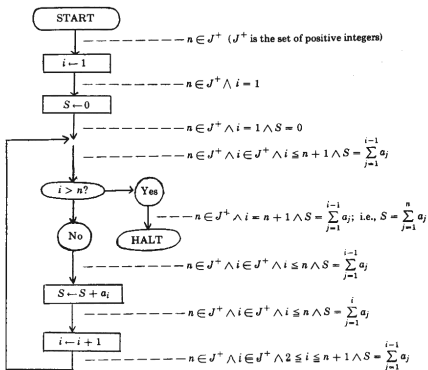


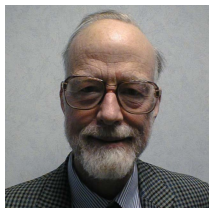
FIGURE 1. Flowchart of program to compute $S = \sum_{j=1}^n a_j$ ($n \geq 0$)

Then, by **induction on the number of commands** executed, one sees that if a program is entered by a connec(on whose associated proposition is then true, it will be left (if at all) by a connection whose associated proposition will be true at the time. By this means, we may **prove certain properties of programs**, ...

Floyd-Hoare Logic: Axioms for Programs

Hoare Triples:

$\{\text{Pre-Condition}\} \text{ Program } \{\text{Post-Condition}\}$



Sir C.A.R. Hoare

- Assignments:

$$\frac{}{\{Q[x/e]\} x := e \{Q\}}$$

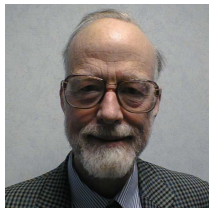
- Composition:

$$\frac{\{P\} S \{Q\} \quad \{Q\} T \{R\}}{\{P\} S; T \{R\}}$$

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Allows us to prove programs correct!

Dijkstra's Predicate Calculus

What *effect* does an instruction have on an assertion?

$$\{x < 10\} \quad x := x + 1 \quad \{?\}$$



Edsger W. Dijkstra

- Strongest Postcondition:

$$\begin{aligned} \text{sp}(x := e, P) = \\ \exists x_0 . x = e[x/x_0] \wedge P[x/x_0] \end{aligned}$$

where x_0 is the “old” value of x

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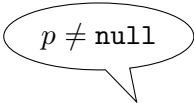
■ Example:

$$\begin{aligned} \text{sp}(x := x + 1, (x < 10)) = \\ \exists(x_0 . x = x_0 + 1) \wedge (x_0 < 10) \end{aligned}$$

Formalisms for Assertions and Specifications



$x \geq 10$

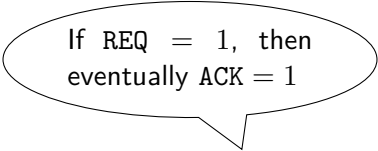


$p \neq \text{null}$

Questionnaire:

- In **which language** are assertions written?
- When do assertions have to hold?
- If all assertions hold, is the program correct?

Limitations of Assertions



If REQ = 1, then
eventually ACK = 1

Questionnaire:

- Can this be expressed as an assertion in C or Java?
- Can we use testing to find such a violation?
- How can this assertion be violated?

Temporal Logic



Amir Pnueli

Linear Temporal Logic

- Temporal operators
 - always
 - eventually
- Describes how executions evolve

Temporal Logic



Amir Pnueli

Linear Temporal Logic

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$AG (REQ \Rightarrow F ACK)$

Model Checking



Edmund Clarke
Allen Emerson
Joseph Sifakis

Basic idea:

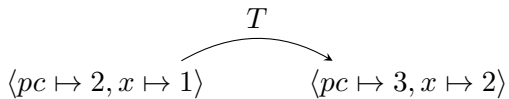
- Assertions in **temporal logic**
- Programs with finite state space
- *models* instead of programs
- all reachable states are inspected!
- also works for concurrent models

T

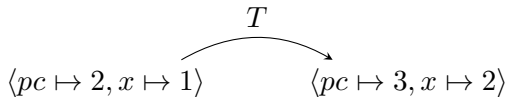
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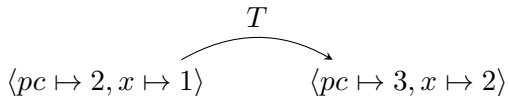


T



(T : operational semantics of program or circuit)

T



(T : operational semantics of program or circuit)

The **Model Checking** problem:

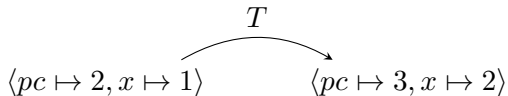


“starting states”



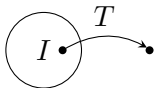
“bad states”

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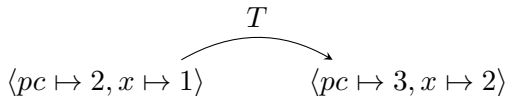


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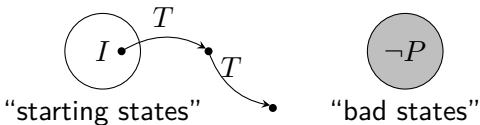
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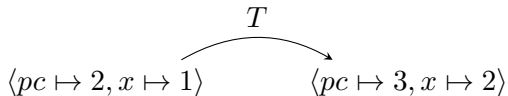


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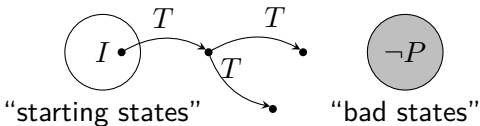


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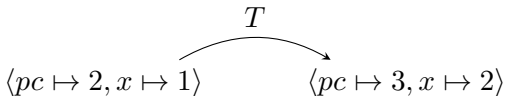


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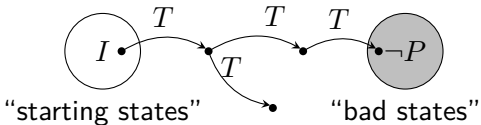


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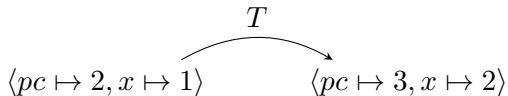


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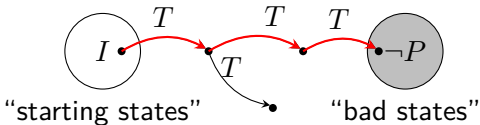


T



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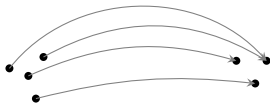
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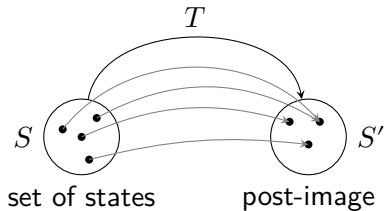


State Space Explosion

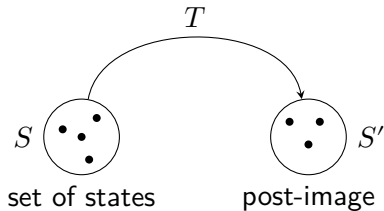
Why explore states one by one?



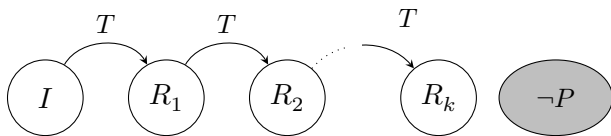
Why explore states one by one?



Why explore states one by one?



$$S' = T(S) \stackrel{\text{def}}{=} \{s' \mid T(s, s') \wedge s \in S\}$$



How do we efficiently represent sets of states?



Ken McMillan

Basic idea:

- use logic to represent states
- implementation: SMV model checker

Logical formulas to represent states

V
⏟
program variables,
registers, latches,
signals, ...

Logical formulas to represent states

$$F(V)$$

$\underbrace{\hspace{10em}}$
program variables,
registers, latches,
signals, ...

Logical formulas to represent states

$(x > 0)$ represents $\{s \mid s(x) > 0\}$

And what about transitions?

Binary Relations!

$$T(V, \underbrace{V'}_{\text{target states}})$$

And what about transitions?

Binary Relations!

$(x' = x + 1)$ represents $\{\langle s, s' \rangle \mid s'(x) = s(x) + 1\}$

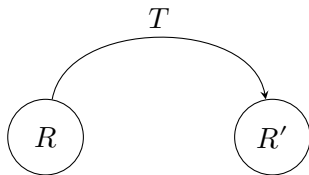
And what about transitions?

Binary Relations!

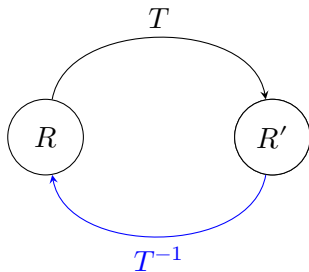
$\underbrace{(x' = x + 1)}_{x++}$ represents $\{\langle s, s' \rangle \mid s'(x) = s(x) + 1\}$



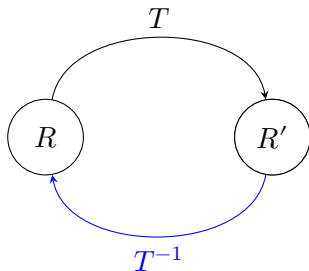
R



$$R'(V') \stackrel{\text{def}}{=} \exists V. R(V) \wedge T(V, V')$$

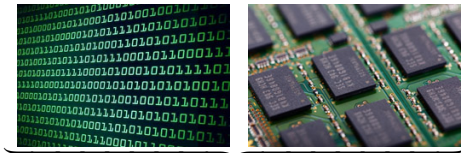


$$\begin{array}{l}
 R'(V') \\
 R(V)
 \end{array}
 \begin{array}{l}
 \stackrel{\text{def}}{=} \\
 \stackrel{\text{def}}{=}
 \end{array}
 \begin{array}{l}
 \exists V. \quad R(V) \quad \wedge \quad T(V, V') \\
 \exists V'. \quad \quad \quad \quad \quad T(V, V') \quad \wedge \quad R'(V')
 \end{array}$$



$$\begin{array}{l}
 R'(V') \stackrel{\text{def}}{=} \exists V. R(V) \wedge T(V, V') \\
 R(V) \stackrel{\text{def}}{=} \exists V'. T(V, V') \wedge R'(V')
 \end{array}$$

(Note the similarity to strongest postcondition)



T

(transition relation)

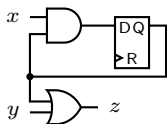

```
1: if (x>0) {  
2:   x = x - 1;  
3: } else {  
4:   x = x + 1;  
5: }
```



T

(transition relation)

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1:  if (x>0) {  
2:    x = x - 1;  
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T

(transition relation)

```
1:  if (x>0)
2:    x = x - 1;
3:  else
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5:  assert (x≥0);
```

$T(\langle pc, x \rangle, \langle pc', x' \rangle)$

$\wedge \left(\right)$

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$T(\langle pc, x \rangle, \langle pc', x' \rangle) \stackrel{\text{def}}{=}$

$$\wedge \left((pc = 1) \wedge (x > 0) \Rightarrow (pc' = 2) \wedge (x' = x) \right)$$

```

1:  if (x>0)
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$T(\langle pc, x \rangle, \langle pc', x' \rangle) \stackrel{\text{def}}{=}$

$$\wedge \left(\begin{array}{l} (pc = 1) \wedge (x > 0) \Rightarrow (pc' = 2) \wedge (x' = x) \\ (pc = 1) \wedge \neg(x > 0) \Rightarrow (pc' = 4) \wedge (x' = x) \end{array} \right)$$

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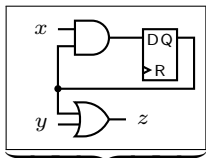
```

$$T(\langle pc, x \rangle, \langle pc', x' \rangle) \stackrel{\text{def}}{=}$$

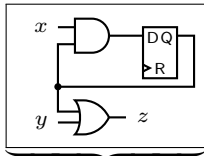
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$$P(V) \stackrel{\text{def}}{=} (pc = 5) \Rightarrow (x \geq 0)$$

$$I(V) \stackrel{\text{def}}{=} (pc = 1)$$



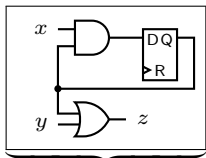
$T(V, V')$



$T(V, V')$

def

$$(Q' \Leftrightarrow (x \wedge Q)) \wedge (z \Leftrightarrow (y \vee Q))$$



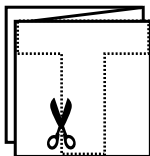
$T(V, V')$

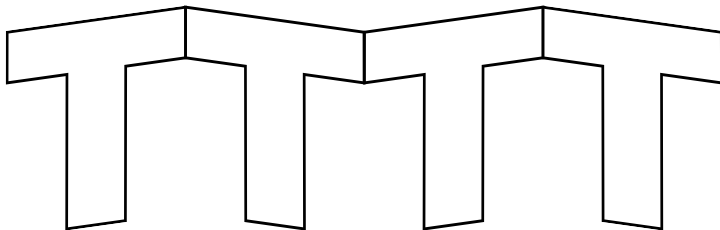
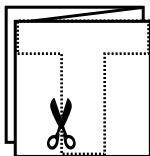
$\stackrel{\text{def}}{=}$

$$(Q' \Leftrightarrow (x \wedge Q)) \wedge (z \Leftrightarrow (y \vee Q))$$

$$P(V) \stackrel{\text{def}}{=} z$$

$$I(V) \stackrel{\text{def}}{=} Q$$





The C Bounded Model Checker (CBMC)



Daniel Kröning

- Checks C programs for assertion violations
- Checks only k loop iterations
- Converts T into propositional logic

<https://www.cprover.org/cbmc>
(and that's where our journey started)

Course Outline

- Part 1: Assertions and Testing
 - Programming and Reasoning with Assertions
 - Testing and Coverage Metrics
 - Automated Test-Case Generation
 - Part 2: Logic and Reasoning
 - Propositional Logic (and SAT Solvers)
 - First-Order Logic (and SMT Solvers)
 - Hoare Logic
 - Temporal Logic
 - Part 3: Automated Verification
 - SMV (Symbolic Model Checking)
 - SPIN (Partial Order Reduction)
 - Bounded Model Checking of C Programs
- } March
- } April
- } May

Lecture, Exercises and Exam

- Lectures: Wednesday and Friday, 9:30am-11am
 - Recordings on LectureTube (see TUWEL)
- VU = lecture + exercises
 - Application of verification and testing tools
 - Pencil & paper homeworks
 - Exercises form 50% of the grade
- 3 exercises (TUWEL)
 - Assertions/Testing/Coverage:
Released March 22, due April 24
 - Hoare Logic and BMC:
Released April 24, due May 24
 - Temporal Logic & Automated Reasoning:
Released May 08, due May 29
- Written Exams (in-person):
 - June 12, 9:00am to 11:00am
 - end of September/beginning of October